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Silicon microdisk-based full adders for optical computing

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Due to the projected saturation of Moore's law, as well as the drastically increasing trend of bandwidth with lower power consumption, silicon photonics has emerged as one of the most promising alternatives that has attracted a lasting interest due to the accessibility and maturity of ultra-compact passive and active integrated photonic components. In this Letter, we demonstrate a ripple-carry electro-optic 2-bit full adder using microdisks, which replaces the core part of an electrical full adder by optical counterparts and uses light to carry signals from one bit to the next with high bandwidth and low power consumption per bit. All control signals of the operands are applied simultaneously within each clock cycle. Thus, the severe latency issue that accumulates as the size of the full adder increases can be circumvented, allowing for an improvement in computing speed and a reduction in power consumption. This approach paves the way for future high-speed optical computing systems in the post-Moore's law era.

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With the continuous shrinking of transistors and on-chip metal interconnects, the power consumption and transmission bandwidth of silicon electronics have been approaching the inevitable limits [1,2]. The exponentially increasing bandwidth requirements for modern computing demand a brand-new generation of alternative techniques to continue Moore's law. Silicon photonics is believed to be one of the promising alternatives due to its potential of using unique properties of light on chip, as well as compatibility with the complementary metal–oxide semiconductor (CMOS) fabrication process [3].

Electro-optic (EO) logic gates and modules [4–6], as the building blocks of optical computing, have gained intensive attention recently because of the accessibility and maturity of abundant compact optical components, such as EO switches or modulators [7,8], interconnects [9–11], and photodetectors (PDs) [12]. Various silicon-based optical logic devices have been proposed and demonstrated experimentally, showing the potential for realizing future chip-based high-speed and low-power consumption optical computing [13–15].

In this Letter, we propose a new design of an EO full adder on the silicon-on-insulator (SOI) platform, where each carry bit ripples to the next full adder directly through single-mode optical waveguides. Thus, the electrical latency caused by the relatively low speed of on-chip electrons can be drastically reduced. Every bit of this full adder utilizes two silicon microdisk resonators. To demonstrate the proposed architecture, a 2-bit thermal-optical (TO) full adder is experimentally demonstrated as a proof of concept with some computation functions demonstrated. The performance projection of the high-speed full adder based on p-n junction devices is presented at the end. A high-speed optical computing chip will be further demonstrated in the future.

As one of the crucial parts in many processors, especially in arithmetic logic units (ALUs), a full adder plays a significant role in computing [16]. It is a combinational logic circuit to perform the addition of three binary digits, which usually functions as a component in a cascade of adders, adding 8-, 16-, 32-, or 64-bit binary numbers. A 1-bit full adder adds three 1-bit numbers A, B, and C (C_{in}), where A and B are the operands, and C is a bit carried in from the previous less significant stage. Two outputs are the carry (C_n) and the sum (S_n) [17]. Then the relationship between these inputs and outputs can be summarized by

$$C_n = (A_n \oplus B_n) \cdot C_{n-1} + A_n \cdot B_n = P_n \cdot C_{n-1} + G_n, \quad (1)$$

$$S_n = C_{n-1} \oplus (A_n \oplus B_n) = C_{n-1} \oplus P_n, \quad (2)$$

where $P_n = A_n \oplus B_n$ (propagate), and $G_n = A_n \cdot B_n$ (generate). Figure 1(a) shows the logic diagram for a 2-bit electrical full adder, where the previous carry bit ripples to the next bit of the full adder.

Obviously, the carry signals C_{n-1} and C_n are the only ones that travel from one bit to the next, intrinsically costing a ripple-carry full adder a lot of time to wait for the carry bit to be calculated from the previous bit of the full adder before proceeding to the next bit. To be specific, the total delay for the n-bit electrical full adder can be expressed as $t_e = t_{dr} + n \times t_{epb}$, where t_{epb} denotes the delay for each bit, and t_{dr} means the time for generating P and G, since all P and G signals can be generated simultaneously. Typically, t_{epb} lies in the range of several picoseconds to tens of picoseconds [18,19]. As a result, it leads to relatively larger latency in the electronics as n increases due to the serialization of the propagation delay.

In contrast to electronic computing, light travels much faster on a chip and has immunity to the distributed capacitance and resistance. For example, it only takes about 0.14 ps for light to go through a 10 μm long silicon waveguide in the SOI platform. Therefore, an optical approach is adopted here to replace the critical path of the electrical full adder to transfer the carry signal from one bit to the next, as shown in Fig. 1(b). The optical carry signal is first separated into two parts. One small portion (~1%) is fed into a PD and transferred into electrical signals before going through an XOR gate to generate the sum signal for the current bit. The other one is first modulated by an EO modulator with a P signal applied and then merges into a combiner to generate the carry signal for the next bit. On the other hand, an optical continuous wave (CW), denoted as λ, is also injected into the full adder. At each bit, a small portion of the CW light is dropped by a splitter and fed into a G-signal-controlled EO modulator, followed by the combiner. This portion is fine-tuned to ensure that the light intensities at two arms before combining are equal. Finally, the equation of this optical part can be written as

$$C_n = P_n \cdot C_{n-1} + G_n \cdot \lambda. \quad (3)$$

Due to the much faster propagation speed of light, it allows the P and G signals to be applied to the modulators simultaneously within every clock cycle. The total delay for this EO full adder can be expressed as $t_o = t_{dr} + t_{sw} + n \times t_{opb}$, where t_{dr} denotes the switch time for generating P and G, t_{sw} is the switching time of the EO modulator, and t_{opb} represents the propagation delay for each bit. Since $t_{opb} \ll t_{epb}$, the latency for the EO full adder can be drastically reduced as the bit size increases.

Microdisk modulators with small footprints and low power dispassion are adopted here as the EO modulators for our proposed full adders for computation so as to achieve a compact, high-speed, and low-power-consumption (power/bit) EO carry-ripple full adder [20]. A 2-bit full adder is discussed herein as a simple example of the scalability. Because there is no carry signal going into the first bit, that is, $C_0 = 0$, we can easily obtain the following carry signals by $C_1 = G_1\lambda$ and $C_2 = C_1P_2 + G_2\lambda$. Thus, the design can be simplified and redrawn accordingly, shown as Fig. 2(a). First, the light is coupled into the full adder through a grating coupler [21] and then split into two parts, serving as the targeted λ for the first and second bit, respectively. After being modulated by several microdisks, light beams from two arms will merge through a combiner to generate the final carry signal. All these operands are applied simultaneously. The operating wavelength is set at the center of the resonance spectrum of these unbiased microdisks, generating an optical "0" at "0" electrical input, as shown

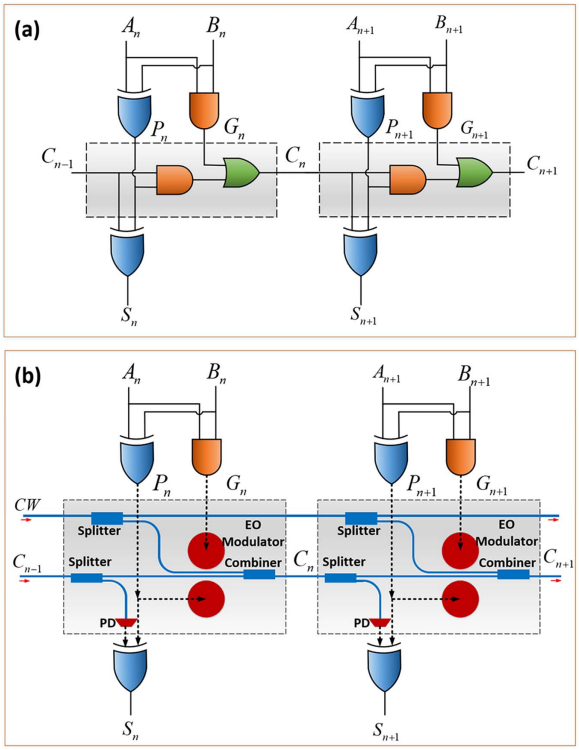

Fig. 1. (a) Schematic diagram of a conventional 2-bit carry-ripple electrical full adder. (b) Schematic of the proposed EO full adder. The critical path transferring carry signals is implemented by optical components and, thus, the signals can be processed all the way through by light with less latency. The driving signals can be applied simultaneously to the EO modulators, and a small portion of the light is dropped off to generate sum signals at each bit.

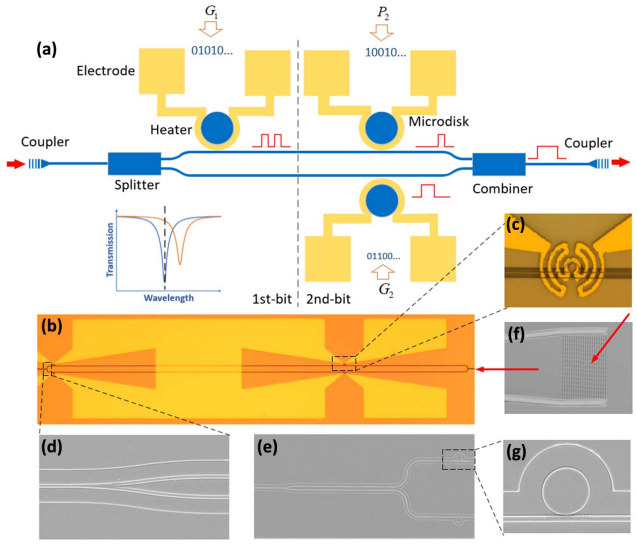

Fig. 2. (a) Schematic diagram of a 2-bit full adder. The inset shows that the induced resonance shift generates the optical "1" and "0." (b, c) Microscope photograph of the 2-bit TO full adder and zoom-in pictures of metallic heaters. (d)–(g) SEM pictures of the splitter/combiner, the combination of splitter and modulators, the grating coupler, and a microdisk with a radius of 2.5 μm.

in the inset in Fig. 2(a). When one applies electrical currents into the modulators, these resonance spectra will redshift due to the carrier dispersion effect or thermo-optic effect [22,23] of silicon and, therefore, let the light go through to generate the optical "1." Here a 2-bit TO full adder is demonstrated as a proof of concept. It should be noted that these thermal modulators can be perfectly replaced by EO modulators to test high-speed performance.

A 2-bit full adder was fabricated on a SOI platform, as shown in Fig. 2(b). The waveguide is 450 nm in width and 220 nm in height. Gold micro-heaters have the thickness of 140 nm with a separation layer of 1.5 μm SiO_2 between the heaters and waveguides. All the microdisks, including a redundant one called the backup microdisk, have radii of 2.5 μm with a gap of 100 nm between the microdisk and the bus waveguide. The quality factors of these microdisks are $\sim 2 \times 10^4$. An amplified spontaneous emission source and an optical spectrum analyzer were first used to align the wavelengths of the three microdisks. After the alignment, the source was switched to a tunable laser. The light beam was fed into the chip through grating couplers and then coupled out to a PD which was connected to an oscilloscope. Finally, pseudorandom non-return-to-zero sequences were applied independently to these EO modulators which function as the logic gates. The results of the device operating at 2.56 kbs^{-1} are shown in Fig. 3. Apparently, this TO full adder shows the function of adding two 2-bit operands A_1A_2 and B_1B_2 and, finally, coming up with the sum S_1S_2 with the carry C_2, as depicted in Fig. 3(a). Since C_0 is 0, one can regard this 2-bit full adder as either two cascaded full adders with zero input or a half-adder followed by a full adder, as shown in Fig. 3(b). All these input digital signals, as well as the sum signals, can be derived from the these carry signals simultaneously by electrical circuits, for example, a field-programmable gate array or integrated CMOS circuits [24]. Figure 3(c) shows the results for the final carry signal at different combinations of inputs, which turned out to be completely consistent with the truth table listed in Fig. 3(d). As can be seen, for example, when G_1 equals 1, which means that there is a carry signal from the first bit, C_2 is equal to the addition of P_2 and G_2. When G_1 is 0, ideally the result of C_2 will be the same as G_2 because no light will go through the second microdisk in the upper arm in Fig. 2(a). However, in the experiment, because of the finite extinction ratio, a little remaining light will still travel through the second bit, acting like dark current. Therefore, three voltage levels appear in Fig. 3, which may make the 0 and 1 levels more confusing. Nevertheless, it can be easily solved by setting a threshold detection between the highest level and the middle one. A modulator with a larger extinction ratio will help to diminish this phenomenon.

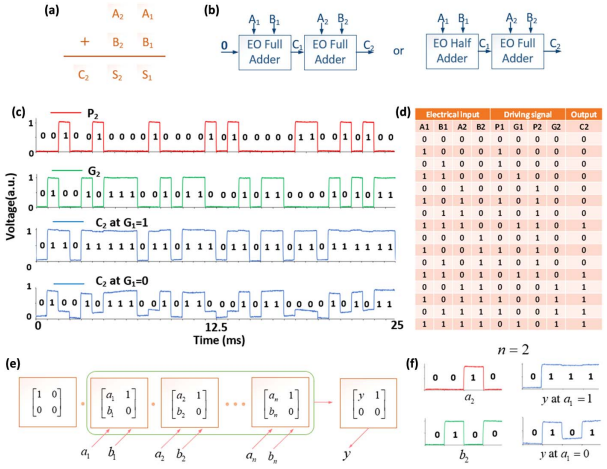

Fig. 3. (a) Function of a 2-bit full adder. (b) Schematic diagram of two approaches of realizing 2-bit full adders. (c) G1, P2, and G2 are the electrical input, and C2 is the optical carry output which is detected by a PD. (d) Truth table for a 2-bit full adder. (e) Expression of a matrix multiplication that can be implemented by the proposed structure. (f) Experimental output y.

Besides the function of addition, this structure is also capable of calculating matrix multiplication in a more generic way, noted as

$$\begin{bmatrix} y & 1 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 & 1 \\ b_1 & 0 \end{bmatrix} \begin{bmatrix} a_2 & 1 \\ b_2 & 0 \end{bmatrix} \cdots \begin{bmatrix} a_n & 1 \\ b_n & 0 \end{bmatrix}, \quad (4)$$

where y is the output, and a_i, b_i are the input from each bit. In other words, the process of going through each bit for the light develops a matrix multiplication, as shown in Fig. 3(e). This function plays a significant part in many scalable logic functions, such as subtractors [25] or neural networks [26]. As an example, in our case of $n = 2$, the expression will be a multiplication of the first three matrices. The results are shown in Fig. 3(f). Note that the input of b_1 is not listed in the figure which is because the result is independent of b_1. Finally, we can have the matrix calculated all at once. For example, with the input of $(a_1, a_2, b_1, b_2) = (0, 1, 0, 1)$, the output y turns out to be 1 after going through the whole matrix calculation. The multi-level 0s are also caused by the finite extinction ratio abovementioned. This EO hybrid computing method can also extend to many other logic modules, for example, fundamental logic building blocks such as multipliers and shifters, as well as other more complicated systems such as neural networks [4].

The performance of the proposed adder is highly dependent on the characteristics of modulators. Many kinds of EO modulators have been demonstrated to be operating at the bandwidth of over 50 Gbps [7,27,28], which leads to a relatively small EO switch time t_{sw}. Further, due to the ultra-compact sizes of these modulators, especially the microdisks with a diameter of only about 10 μm, the propagation delay per bit t_{opb} will be shortened to 0.5 ps under the condition that the total length of each bit region is around 40 μm with the help of ultra-compact passive splitters and combiners [29]. Under the scenario of $t_{sw} = 50$ ps and $t_{dr} = 10$ ps, one can obtain the maximum

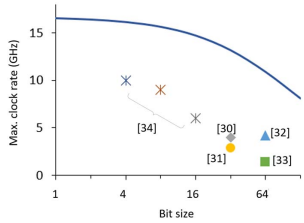

Fig. 4. High-speed performance projection. The blue solid curve represents the maximum clock rate for the EO full adder with high-speed performance projection in theory. Some published data of electrical full adders are also plotted.

operating speed, as shown in Fig. 4. As a comparison, some published data on the clock rate of conventional CMOS electrical full adders or ALUs are also plotted in Fig. 4 [30–34]. Obviously, EO full adders are capable of operating much faster than conventional full adders in theory. A concern that may limit the scalability and should be taken into consideration is the propagation loss. Though the insertion loss of each modulator can be really small [23], it should be noted that each combiner will intrinsically cause a 3 dB loss due to the mode mismatch between the asymmetric input and output. Therefore, amplifiers should be added into the system when it goes to a high-bit system. One solution is to pump the signal using an off-chip erbium-doped fiber amplifier and then couple the light back to the next bit [24]. Another better solution, in terms of integration, is to utilize hybrid-integrated III-V-on-silicon optical amplifiers [35], which spares the system the trouble of coupling light in and out of the chip. The dynamic power consumption of this EO full adder, as another crucial factor, is largely dependent on the performances of the modulators, such as the modulation bandwidth, insertion loss, and extinction ratio. As mentioned above, an ultralow power "athermal" microdisk modulator only consumes <1 fJ/bit [20], which makes this EO full adder comparable with the traditional electrical full adders in terms of power consumption. It should also be noted that it is achievable to integrate the laser sources, amplifiers, and PDs in a monolithic InP chip to further increase the system integration [36]. In addition, in our experiments, the driving circuits and detecting circuits are realized by off-chip circuits and instruments while, in the future, the co-integrated electronic-photonic chip could provide the capability to combine electrical and optical interconnects using a standard microelectronics CMOS foundry [24].

In conclusion, we proposed a microdisk-resonator-based carry-ripple EO full adder, which utilizes optical components to replace the conventional electrical parts in the critical path to transfer carry signals from one bit to the next. Since the latency of this EO full adder does not accumulate due to the small propagation delay for light on a chip, it will pave the way for the future high-speed optical computing systems. At last, a TO full adder is demonstrated to prove the feasibility and validity before a performance projection of a high-speed EO full adder based on p-n junction microdisk modulators. The proposed logic module could also extend to many other logic modules and networks. Further integration of this full adder with the most advanced techniques needs to be explored to achieve the full advantage of hybrid photonic-electronic systems.

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REFERENCES

1. C. Kachris and I. Tomkos, IEEE Commun. Surv. Tutorials **14**, 1021 (2012).
2. D. Miller, Appl. Opt. **49**, F59 (2010).
3. H. Subbaraman, X. Xu, A. Hosseini, X. Zhang, Y. Zhang, D. Kwong, and R. T. Chen, Opt. Express **23**, 2487 (2015).
4. Q. Xu and R. Soref, Opt. Express **19**, 5244 (2011).
5. R. Soref and J. Hendrickson, Opt. Express **23**, 32582 (2015).
6. J. Hendrickson, R. Soref, J. Sweet, and W. Buchwald, Opt. Express **22**, 3271 (2014).
7. T. Baba, S. Akiyama, M. Imai, N. Hirayama, H. Takahashi, Y. Noguchi, T. Horikawa, and T. Usuki, Opt. Express **21**, 11869 (2013).
8. C. T. Phare, Y.-H. Daniel Lee, J. Cardenas, and M. Lipson, Nat. Photonics **9**, 511 (2015).
9. M. Rakowski, M. Pantouvaki, P. Verheyen, J. De Coster, G. Lepage, P. Absil, and J. Van Campenhout, in *Optical Fiber Communication Conference* (2016), pp. 5–7.
10. Z. Ying, G. Wang, X. Zhang, Y. Huang, H. P. Ho, and Y. Zhang, IEEE Photon. Technol. Lett. **27**, 201 (2015).
11. Z. Ying, G. Wang, X. Zhang, H. Ho, and Y. Huang, Opt. Lett. **40**, 2134 (2015).
12. J. Michel, J. Liu, and L. C. Kimerling, Nat. Photonics **4**, 527 (2010).
13. L. Zhang, J. Ding, Y. Tian, R. Ji, L. Yang, H. Chen, P. Zhou, Y. Lu, W. Zhu, and R. Min, Opt. Express **20**, 11605 (2012).
14. L. Yang, R. Ji, L. Zhang, J. Ding, and Q. Xu, Opt. Express **20**, 13560 (2012).
15. C. Qiu, X. Ye, R. Soref, L. Yang, and Q. Xu, Opt. Lett. **37**, 3942 (2012).
16. G. Li, A. V. Krishnamoorthy, I. Shubin, J. Yao, Y. Luo, H. Thacker, X. Zheng, K. Raj, and J. E. Cunningham, IEEE J. Sel. Top. Quantum Electron. **19**, 95 (2013).
17. S. Kaur, R.-S. Kaler, and T.-S. Kamal, J. Opt. Soc. Korea **19**, 222 (2015).
18. R. Megha and B. R. Vishwanath, Int. Res. J. Eng. Technol. **4**, 1931 (2017).
19. S. L. Gates, G. Merrett, and B. M. Al-hashimi, in *14th International Workshop on Power and Timing Modeling, Optimization* (2015), pp. 936–944.
20. E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. Shah Hosseini, A. Biberman, and M. R. Watts, Nat. Commun. **5**, 4008 (2014).
21. X. Xu, H. Subbaraman, J. Covey, D. Kwong, A. Hosseini, and R. T. Chen, Appl. Phys. Lett. **101**, 031109 (2012).
22. R. A. Soref and B. R. Bennett, IEEE J. Quantum Electron. **23**, 123 (1987).
23. G. Reed, G. Mashanovich, F. Gardes, and D. Thomson, Nat. Photonics **4**, 518 (2010).
24. C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, A. S. Waterman, J. M. Shainline, R. R. Avizienis, S. Lin, B. R. Moss, R. Kumar, F. Pavanello, A. H. Atabaki, H. M. Cook, A. J. Ou, J. C. Leu, Y.-H. Chen, K. Asanović, R. J. Ram, M. A. Popović, and V. M. Stojanović, Nature **528**, 534 (2015).
25. M. Gautam and S. Akashe, in *International Conference on Computer Communication and Informatics (ICCCI)* (2013), pp. 13–16.
26. Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund, and M. Soljacic, Nat. Photonics **11**, 441 (2017).
27. D. J. Thomson, F. Y. Gardes, J. M. Fedeli, S. Zlatanovic, Y. Hu, B. P. P. Kuo, E. Myslivets, N. Alic, S. Radic, G. Z. Mashanovich, and G. T. Reed, IEEE Photon. Technol. Lett. **24**, 234 (2012).
28. D. J. Thomson, F. Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J.-M. Fedeli, and G. T. Reed, Opt. Express **19**, 11507 (2011).
29. Y. Zhang, S. Yang, A. E.-J. Lim, G.-Q. Lo, C. Galland, T. Baehr-Jones, and M. Hochberg, Opt. Express **21**, 1310 (2013).
30. S. Mathew, M. Anders, R. K. Krishnamurthy, and S. Borkar, IEEE J. Solid-State Circuits **38**, 689 (2003).
31. A. T. Tran and B. M. Baas, in *International Conference on Consumer Electronics* (2010), pp. 87–91.
32. R. Zlatanovici, S. Kao, and B. Nikolic, IEEE J. Solid-State Circuits **44**, 569 (2009).
33. U. G. Nawathe, M. Hassan, K. C. Yen, A. Kumar, A. Ramachandran, and D. Greenhill, IEEE J. Solid-State Circuits **43**, 6 (2008).
34. I. Levi, O. Bass, A. Kaizerman, A. Belenky, and A. Fish, in *IEEE International Symposium of Circuits and Systems (ISCAS)* (2012), pp. 3037–3040.
35. S. Keyvaninia, G. Roelkens, D. Van Thourhout, G. H. Duan, M. Lamponi, F. Lelarge, J. M. Fedeli, S. Messaoudene, E. J. Geluk, and B. Smalbrugge, in *IEEE International Conference on Group IV Photonics (GFP)* (2012), Vol. **6**, pp. 222–224.
36. J. S. Fandiño, P. Muñoz, D. Doménech, and J. Capmany, Nat. Photonics **11**, 124 (2017).