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Letter

Electrically Tunable High-Quality Factor Silicon Microring Resonator Gated by High Mobility Conductive Oxide

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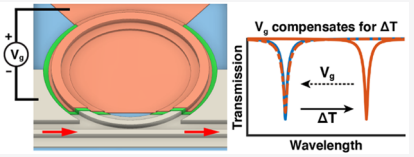
ABSTRACT: Silicon microring resonators play pivotal roles in photonic integration circuits due to the advantages of low power consumption, high bandwidth, and ultracompact size. However, silicon microring resonators also face great challenges to control the working wavelength due to fabrication errors and temperature variation. In this work, we demonstrate an electrically tunable silicon microring resonator driven by a titanium-doped indium oxide/hafnium oxide/silicon metal-oxide-semiconductor capacitor, achieving a high electro-optic tuning efficiency of 130 pm/V with a high quality factor between 11900 and 4700. The high electro-optic tuning efficiency can be used to compensate for the drift of resonance wavelength induced by temperature fluctuation up to 12 K with an extremely low power consumption of 11 pW/nm, which is superior to the conventional thermal tuning.



KEYWORDS: *silicon photonics, microring resonator, transparent conductive oxides, electrical tuning, energy-efficient photonic device*

Microring resonators (MRRs) can serve as multipurpose photonic devices for laser emission, electro-optic (E-O) modulation, add-drop filtering, wavelength conversion, and wavelength division multiplexing (WDM)/demultiplexing.[1−3] Therefore, MRR is one of the most critical devices in photonic integrated circuits with exclusive advantages in terms of high energy efficiency, wide bandwidth, and a small footprint for optical communication and optical computing.[1,4] In silicon photonics, silicon MRR (Si MRR) is often used as a tunable optical filter and an E-O modulator by applying electronic signals.[5] Most reported Si MRRs are driven by reversed PN junctions, which only provide a low E-O tuning efficiency below 40 pm/V.[5−9] However, the resonance wavelength of the Si MRR is easily affected by fabrication errors and fluctuations in temperature due to the high thermo-optic (T-O) coefficient of silicon (1.86×10^{-4} K^{-1}),[10] while the reversed PN junction structure cannot sufficiently compensate the drift. Therefore, a thermal heater is widely used to control the resonance wavelength of Si MRR with the sacrifice of high power consumption (in mW/nm) and the requirement of controlling circuits.[11−13] Recently, metal-oxide-semiconductor (MOS) Si MRR with heterogeneously integrated materials such as III−V, poly-Si, and transparent conductive oxides (TCOs), have been reported with much higher E-O tuning efficiency.[14−16] Of these heterogeneous gate materials, TCOs offer a large plasma dispersion effect and can be easily integrated with silicon photonics by DC- or RF-sputtering.[17,18] For example, our group experimentally demonstrated an indium−tin-oxide (ITO)-gated Si MRR, which achieved an ultrahigh E-O tuning efficiency of 271 pm/V using a narrow microring waveguide with a hafnium oxide (HfO_2) insulator.[19] However, the quality factor (*Q*-factor) is limited to 1000 due to the high optical loss from the ITO gate. In principle, the optical loss can be reduced by high-mobility TCO materials to improve the *Q*-factor of the electrically tunable MRR.[20] Titanium-doped indium oxide (ITiO) is one of the high-mobility TCO materials, which can achieve the high mobility of 105 cm^2 V^{-1} s^{-1} by an optimized RF sputtering process.[21]

In this Letter, we demonstrate an electrically tunable Si MRR with an integrated ITiO/HfO_2/Si MOS capacitor, which has a high E-O tuning efficiency of 130 pm/V with a high *Q*-factor between 11900 and 4700. The high E-O tuning efficiency can be used to compensate for the temperature fluctuation (ΔT) up to 12 K with an extremely low power consumption of 11 pW/nm. Figure 1a shows the three-dimensional (3D) schematic of the electrically tunable MRR with a radius of 6 μm. The ITiO-gated MOS MRR is fabricated on a Si-on-insulator (SOI) substrate with the fabrication flow described in our previous work.[22,23] In contrast to our earlier work,[23] the SiO_2 layer of the MOS capacitor is replaced by a 10 nm HfO_2 to enhance the E-O tuning efficiency.[19] Besides, the thickness of the ITiO gate is reduced to 8 nm to suppress the optical absorption, which covers the active region, as shown in Figure 1b. Figure 1c shows the cross-sectional schematic in the device's active region and the accumulation layers. The Drude model can describe the optical properties of ITiO,[24] and the fundamental device working principle has been discussed in more detail in our previously published work.[19,23] When a

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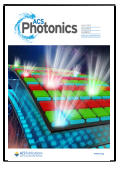

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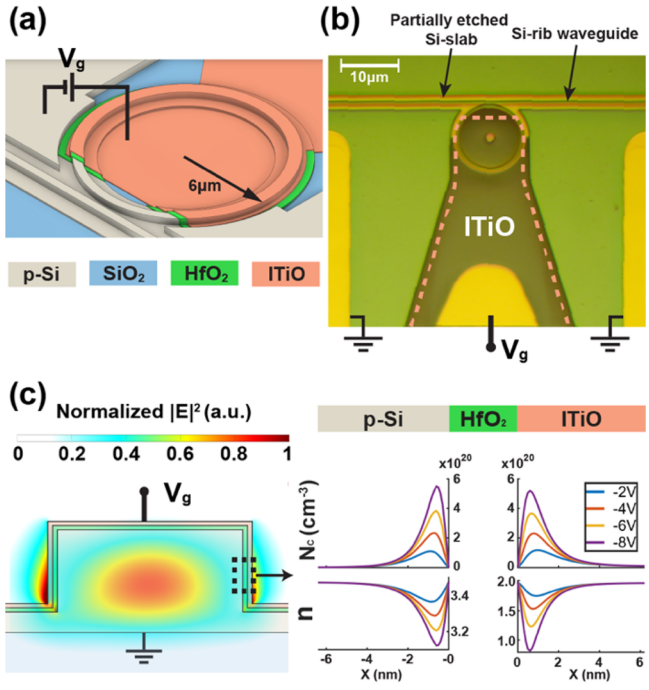

Figure 1. (a) 3D schematic of the ITiO-gated Si MOS MRR. (b) An optical image of the fabricated MRR. The ITiO gate is highlighted by the dashed line and covers the active region of the MRR except the coupling region to the bus waveguide. (c) The cross-sectional schematic and the example of optical mode profile ($|E|^2$) at $V_g = -3$ V in the active region. The negative V_g induces carrier accumulation and refractive index modulation.

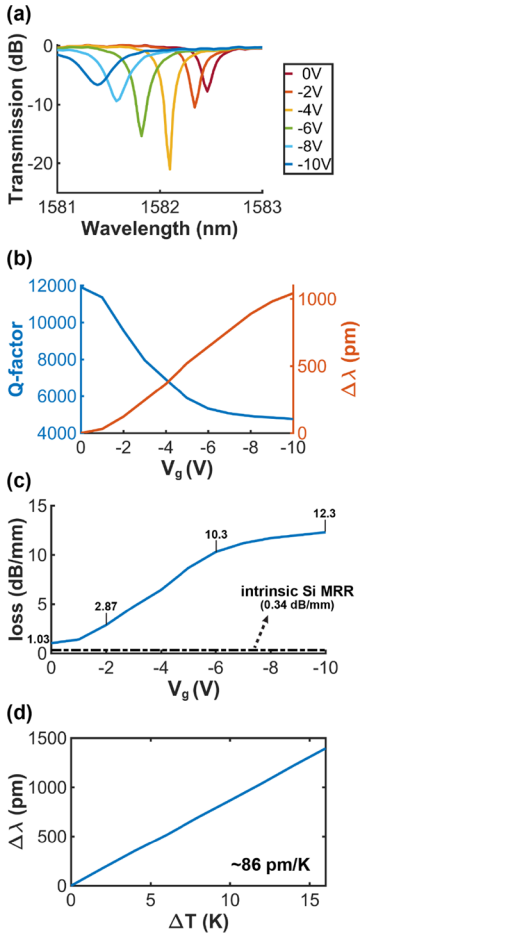

Figure 2. (a) Normalized transmission spectra of the ITiO-gated MOS Si MRR with different V_g values. (b) Experimentally measured Q-factor (blue line, left y-axis) and $\Delta\lambda$ (red line, right y-axis). (c) Blue curve: the loss in ITiO-gated MOS Si MRR, including both waveguide bending and optical absorption losses. Dashed line: the bending loss of the intrinsic Si MRR extracted from the passive Si MRR with a Q-factor of 13000. (d) Experimental $\Delta\lambda$ caused by ΔT without gate voltage ($V_g = 0$ V).

negative bias (V_g) is applied, electrons accumulate in the ITiO layer, which causes the refractive index to change in the accumulation layer.[25] Similarly, the refractive index change in the Si accumulation layer is induced by the holes accumulated with the negative V_g.[26] The resonance wavelength of the MRR has a blue shift due to the changes of refractive indices in ITiO and Si accumulation layers.

Figure 2a shows the transmission spectra of the tunable MRR versus the gate voltage V_g at room temperature. When a negative V_g is applied to the ITiO gate, the resonance wavelength experiences a blue shift. The initial tunable MRR ($V_g = 0$ V) is designed at the overcoupling condition, so the extinction ratio (ER) increases until V_g goes to -4 V. The $\Delta\lambda$ and Q-factor at each V_g are measured and plotted in Figure 2b. The $\Delta\lambda$ is almost linearly proportional to the V_g from -2 V to -6 V, and it has a high average E-O tuning efficiency of 130 pm/V. When the negative V_g increases, it induces higher optical absorption loss and causes the Q-factor to degrade gradually from 11900 to 4700. Since the Q-factor depends on the loss of the MRR,[1] it can be used to derive the loss of the optical waveguide in ITiO-gated MRR. The dashed line in Figure 2c is obtained from the passive Si MRR and it shows that the waveguide bending loss of the MRR is 0.34 dB/mm based on a Q-factor of 13000. Additionally, the blue curve shows the total loss of the ITiO-gated MRR waveguide, including both the bending loss and optical absorption. It increases from 1.03 to 12.3 dB/mm due to the increased optical absorption as V_g rises.

The thermal effect of the MRR is measured by increasing the substrate temperature, which is controlled by a temperature controller (Thorlabs-TED200C) with a TEC element (Thorlabs-TEC J6), and it has a T-O tuning efficiency of 86 pm/K, as shown in Figure 2d. The plasma dispersion effect induced by the gate voltage can be used to compensate for the T-O effect. The solid lines in Figure 3a show that the resonance wavelength has a red shift when we increase the substrate temperature. With negative gate voltages, V_g, the resonance wavelength is blue-shifted against the red-shift induced by ΔT, as shown in the dashed lines of Figure 3a, resulting in stabilized working wavelength even as the temperature varies. The inset of Figure 3a plots the required V_g to compensate for ΔT, and the thermal tuning range of this MRR is around 12 K. Since the plasma dispersion effect of ITiO is accompanied by the increase of optical absorption, using the gate voltage to compensate the temperature drift will simultaneously induce variations of ER and Q-factor, which are plotted in Figure 3b. The ER of the MRR can increase after the compensation due to the overcoupling condition of the initial MRR ($V_g = 0$ V). Besides, it can almost have the same ER as the initial MRR ($V_g = 0$ V, $\Delta T = 0$ K) when it compensates for 12 K temperature drift. The Q-factor is gradually decreasing because of the incremental optical absorption loss.

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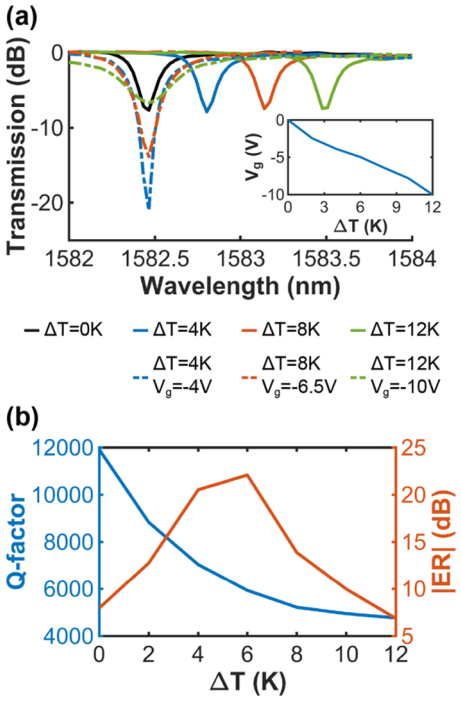

Figure 3. (a) Normalized transmission spectra of ITiO-gated MOS Si MRR with different ΔT and compensated V_g. The solid lines are the spectra red-shifted by ΔT. The dashed lines are the spectra relying on V_g to compensate for the ΔT. Inset: the required V_g to compensate for $\Delta\lambda$ caused by ΔT. (b) After the compensation by applying V_g, and the change of Q-factor (blue line, left y-axis) and ER (red line, right y-axis).

We measured the leakage current of the ITiO/HfO_2/Si MOS capacitor and plotted it in Figure 4. It has an average

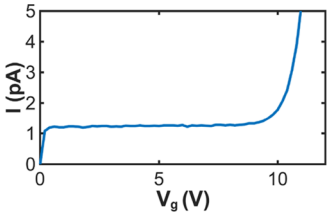

Figure 4. Leakage current of ITiO/HfO_2/Si MOS capacitor as a function of V_g.

leakage current of 1.2 pA and an average E-O tuning efficiency of 105 pm/V at V_g from 0 to −10 V. It has a tuning power efficiency of 11 pW/nm, which is much more efficient than thermal tuning in the range of several mW/nm. From Figure 4 we also see this tunable MRR has a breakdown voltage of around −10 V. Therefore, we can have an adequate electrical tuning range from 0 to −10 V, and it can compensate for ΔT up to 12 K with low power consumption. However, we still need to further enhance the E-O tuning efficiency to compensate for ΔT up to 20 K, which is the suggested temperature tuning range for silicon photonics to be used in on-chip optical communication.[27,28] By narrowing the MRR's waveguide to 300 nm, as discussed in our previous work, we can achieve higher E-O tuning efficiency,[19] and it potentially can compensate ΔT up to 30 K.

In conclusion, we demonstrated an electrically tunable ITiO-gated MOS Si MRR. It achieved a high E-O tuning efficiency of 130 pm/V with a high Q-factor of 11900. This tunable MRR can be used to compensate the temperature drift up to 12 K while still maintaining a high Q-factor above 4700. In addition, it has a high power efficiency of 11 pW/nm, which is much more efficient than the conventional thermal tuning of several mW/nm. With a narrower waveguide width of MRR, we expect it to offset the ΔT up to 30 K. Therefore, the tunable ITiO-gated MOS Si MRR can provide high energy efficiency for on-chip WDM communication on a silicon photonics platform.

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Notes

The authors declare no competing financial interest.

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