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One-Volt Silicon Photonic Crystal Nanocavity Modulator with Indium Oxide Gate

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The ever-increasing global network traffic requires high level of seamless integration between optical interconnect systems and complementary metal-oxide-semiconductor (CMOS) circuits. Therefore, it brings stringent requirement for future electro-optic (E-O) modulators, which should be ultra-compact, energy efficient, high bandwidth and in the meanwhile, able to be directly driven by the state-of-the-art CMOS circuits. In this manuscript, we report a low-voltage silicon photonic crystal nanocavity modulator using an optimized metal-oxide-semiconductor (MOS) capacitor consisting of $\text{In}_2\text{O}_3/\text{HfO}_2/\text{p-Si}$ stacked nanostructure. The strong light-matter interaction from the accumulated free carriers with the nanocavity resonant mode results in holistic improvement in device performance, including a high tuning efficiency of 250pm/V and an average modulation strength of 4dB/V with a moderate Q factor of $\sim 3,700$ and insertion loss of $\sim 6\text{dB}$ using an ultra-short electrode length of only 350nm. With one-volt driving voltage over a capacitive loading of only 13fF, the silicon photonic nanocavity modulator can achieve more than 3dB extinction ratio with energy consumption of only 3fJ/bit. Such low-voltage, low capacitance silicon nanocavity modulator provides the feasibility to be directly driven by a CMOS logic gate for single-chip integration.

OCIS codes: (130.4110) Modulators; (130.5296) Photonic crystal waveguides; (200.4650) Optical interconnects; (230.5298) Photonic crystals; (250.0250) Optoelectronics; (250.7360) Waveguide modulators.

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1. INTRODUCTION

The exponentially growing global network traffic creates an unceasing driving force to upgrade the optical interconnect systems [1]. Silicon photonics offers the great potential to increase the integration level of photonics systems with CMOS circuits, and ultimately monolithic integration that can significantly enhance the bandwidth of the optical interconnects and reduce the cost and energy consumption by orders of magnitude. To achieve this goal, it

requires future silicon E-O modulators, the basic building block for optical communication systems, to be ultra-compact, high bandwidth and energy efficient. More importantly, the driving voltage of the modulator must be compatible with CMOS driving circuits, ideally directly driven by a CMOS logic gate. For example, 32 nm CMOS technology node requires a peak-to-peak voltage swing around 0.9V [2] and this value will further scale down with more advanced CMOS technology. However, because of the weak plasma dispersion effect of silicon, there is always a trade-off between the driving voltage and modulation length. Conventional Mach-Zehnder interferometer (MZI) based silicon E-O modulators occupy large footprints in order to operate in low voltage [3, 4], which are not suitable for high density integration. On the other hand, micro-resonator based silicon modulators, such as micro-rings [5, 6] or micro-disk modulators [7, 8], can operate in low voltage due to the high Q-factor ($10^4\sim 10^5$) of the resonator. But such high Q-factor limits the RF operational bandwidth due to the long photon life time. For example, a Q factor above 10^4 will limit the RF bandwidth below 20GHz. So for high-speed resonator based modulators, a moderate Q-factor of a few thousand is desired. Besides, excessive Q-factor also requires heaters with precise feedback circuits to lock the operational wavelength.

In order to bypass the intrinsic limitation of silicon, people are seeking other active materials that can be integrated with the silicon photonics platform, such as graphene [9, 10], transparent conductive oxides (TCOs) [11-14], and phase-change oxide materials [15]. Among them, TCOs, such as indium-tin oxide (ITO) and aluminum-zinc oxide (AZO), well known as transparent electrode materials in display and solar cell industries, have attracted escalating attention due to their strong plasma dispersion effect. The refractive index of TCO materials can experience unit order change by tuning the carrier concentration [16], and TCO also exhibits the unique epsilon-near-zero (ENZ) effect in the telecom wavelength window [17]. People have utilized the ENZ optical confinement effect to build electro-absorption (EA) modulators, such as hybrid plasmonic MOS modulators [11, 12] and PlasMOSor [13]. However, it requires a relatively large driving voltage to accumulate enough carrier in order to turn the TCO materials into ENZ. In our previous work [14], we reported that by building a TCO/oxide/Si MOS capacitor on a photonic crystal nanocavity, we may take full advantage of the real part and imaginary part

modulation of the optical permittivity from both TCO and Si, which enables us to achieve an efficient modulation in a sub-wavelength scale active region. However, the tuning efficiency is limited by the small capacitance density due to the SiO₂ gate insulator layer. In this manuscript, we report a low-voltage TCO-gated silicon photonic crystal nanocavity modulator using optimized MOS capacitor consisting of indium oxide (In₂O₃)/HfO₂/p-Si stacked nanostructure. Using the 10nm thick high-k dielectric material, HfO₂, as the gate insulator layer greatly increases the capacitance density in the active region, bringing unprecedented energy efficiency. We experimentally demonstrate a high resonance tuning efficiency of 250 pm/V. The device exhibits an average modulation strength of 4dB/V for a moderate Q factor of ~3,700. The 3dB driving voltage is reduced to less than 1V on a 13 fF gate, which can be directly driven by CMOS logic gates without any additional signal amplification. Besides, the device also preserves the feasibility to scale down the driving voltage by reducing the thickness of the gate oxide layer. Since the active volume of our nanocavity modulator is 10~50x smaller compared with micro-ring or micro-disk modulators, our modulator should be more efficient in thermal tuning. Also the moderate Q-factor makes the device quite tolerant to temperature variation although a thermal heater may still be needed to lock the operational wavelength.

2. Design

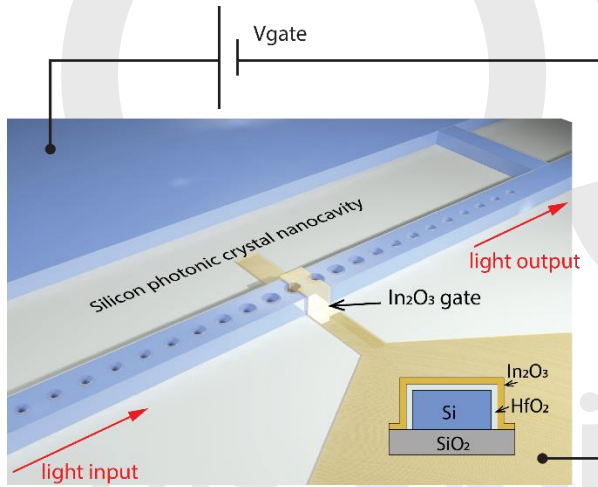


Fig. 1. 3D Schematic of the photonic crystal nanocavity modulator. Inset: cross section schematic of the In₂O₃/HfO₂/p-Si film stack in the active region.

Fig 1a shows the schematic of the photonic crystal nanocavity E-O modulator. A photonic crystal nanocavity is created on a strip silicon waveguide with 500 nm in width and 245 nm in height. Two tapered photonic crystal mirror segments are placed back to back, resulting in a zero-length cavity. Each mirror segment consists of 12 air holes with a period of 340 nm. The size of air holes is quadratically tapered from the edge to the center. [21] An In₂O₃/HfO₂/p-Si film stack is formed in the center of nanocavity, forming a MOS capacitor which is the active region of the modulator with cross sectional view shown in the fig 1a inset. Here, the p-Si performs as the semiconductor layer. Two silicon strips are placed 5μm away from the center on each side of the cavity, providing

electrical connection between the silicon cavity and the silicon slab contacted with the metallic electrode. A 10nm thick high-k dielectric, HfO₂, film serves as the gate oxide. On the top, a 20nm thick In₂O₃ film acts as the TCO gate electrode. Here, we choose In₂O₃ as the TCO material instead of previously used ITO, because In₂O₃ offers slightly higher mobility than ITO in our fabrication facility, which can potentially improve the plasma dispersion effect. The total length of the overlapping area is 350 nm. Compared with other high-Q resonators such as micro-ring and micro-disks, photonic crystal nanocavity has more confined mode volume [18, 19]. We simulate the photonic crystal nanocavity modulator based on 3D finite-difference time-domain (FDTD) method. The nanocavity operates in the transverse-electric (TE) mode. The simulation shows an ultra-compact mode volume of 0.049 μm³ (0.25(λ/n)³), which is more than one order of magnitude smaller than the most compact micro-disk resonator [20]. Fig 2a and 2b shows cross sectional and top view of the optical mode profile of the TE cavity mode. Best tuning efficiency of plasma dispersion effect happens when the carrier modulation happens near the region where the optical field has the maximum power. [7] In the photonic crystal nanocavity modulator, this corresponds to the center silicon region (~130 nm wide) between two photonic crystal segments. In our design, we chose the In₂O₃ gating length to be slightly bigger than one period between air holes, majorly due to the consideration of fabrication tolerance. But it still gives us an ultra-small active volume of V_a=0.06 μm³.

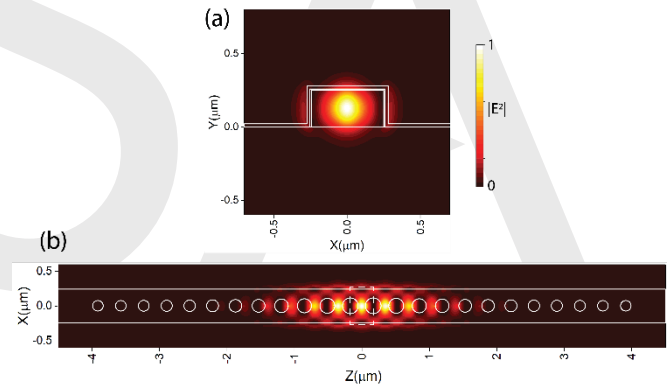


Fig. 2. (a) Cross sectional $|E|^2$ distribution in the center of the photonic crystal nanocavity ($Z=0\mu\text{m}$). (b) $|E|^2$ distribution in the center plane of the photonic crystal nanocavity.

The active region of the photonic crystal nanocavity modulator is driven by a MOS capacitor. A negative bias applied on the In₂O₃ gate produces free carrier accumulation at both the In₂O₃/HfO₂ (electron) and the HfO₂/p-Si (holes) interfaces. We know that the permittivity change caused by the plasma dispersion is proportional to the change of free carrier concentration [14]. A MOS capacitor can easily provide a huge capacitance density using thin high-k gate insulator layer. For example, a MOS capacitor with 10 nm HfO₂ gate oxide layer has a large capacitance density of 22.1 fF/μm². As comparison, the capacitance density for PN junction with doping level of 10¹⁸ cm⁻³ is only ~1.5 fF/μm². Especially for our photonic crystal nanocavity modulator, it is actually a 3D-MOS capacitor. Free carriers can accumulate at all the surrounding interfaces (side wall interfaces in four in-plane directions and the

top interface). A large capacitance (C) can be achieved in a very small active volume (V_a). We simulate the capacitance of the modulator through commercially available software (ANSYS HFSS) based on finite element method (FEM). The simulation gives a gate capacitance of 13 fF, which corresponds to a capacitance over active volume ratio of $C/V_a=216 \text{ fF}/\mu\text{m}^3$.

3. RESULTS AND DISCUSSION

A. Fabrication

The modulator fabrication process starts with a p-type silicon-on-insulator (SOI) wafer with a silicon layer thickness of 250 nm and the buried oxide layer thickness of 3 μm . First, the SOI wafer is uniformly implanted with 34 keV B⁺ ions at a flux of $2 \times 10^{13} \text{ ions cm}^{-2}$ to lightly dope the silicon layer and reduce the resistivity. Then, the silicon waveguide, photonic crystal cavity and grating couplers are patterned by diluted ZEP520A resist using electron beam lithography (EBL), followed by a reactive ion etching (RIE) process to etch through the silicon layer. We found that the resonance peak of our fabricated device shifts to shorter wavelength compared with the design value. The dimension of the actual fabricated device is 5% larger than the designed value as listed above. A 10nm thick SiO₂ layer is then formed by thermal oxidation at 1000°C in order to smooth the etching surface (to improve the Q factor) and also activate the dopants. After etching the SiO₂ layer by buffered oxide etchant (BOE), a 10nm thick HfO₂ is deposited using atomic layer deposition (ALD). Next, Al and Au electrode pads are patterned by contact photo lithography, thermal evaporation and lift-off process, contacting with the Si and In₂O₃ layer respectively. Before metal evaporation, the overlapped HfO₂ layer is removed by BOE. The sample is then annealed at 475 °C to form Ohmic contact between Al and Si. Finally, the 20 nm In₂O₃ gate layer is patterned by a second time EBL with ZEP resist followed by room-temperature RF sputtering and lift-off process. Fig 3 (a)-(c) show the scanning electron microscopy (SEM) images of one fabricated device.

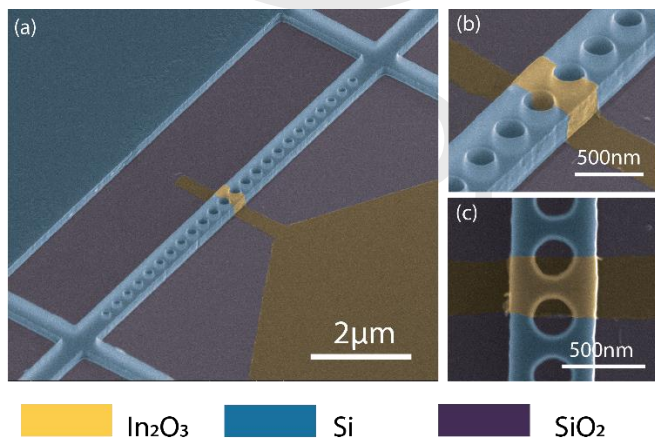


Fig 3. (a) Colored scanning electron micrograph (SEM) of one fabricated photonic crystal nanocavity modulator. (b) Zoomed-in SEM of the MOS structure in the active region of the nanocavity modulator. (a) and (b) are taken with the sample tilted at 45°. (c) Top view SEM of the active region of the nanocavity modulator.

B. Optical characterization and E-O modulation

We perform optical and E-O modulation characterization of the device. Light is coupled into and out of the silicon waveguide through grating couplers from optical fibers with a 10° tilted angle. At the input side, a polarization-maintaining fiber is used to maintain the TE mode polarization controlled by a polarization controller. The output light is then coupled into an optical spectrum analyzer. During the E-O testing, a DC voltage is applied onto the top In₂O₃ gate electrode while the bottom silicon waveguide is grounded. Fig 4a shows the plots of the transmission spectra at different applied bias voltages. The spectra are normalized to a straight Si waveguide with same crossing strips as the reference. When no bias applied, a transmission peak with a relative high Q factor of 3,700 is observed at 1545.39 nm. The insertion loss at peak wavelength is ~6dB, which is majorly caused by fabrication errors and waveguide surface roughness. Compared with the transmission spectrum before sputtering the In₂O₃ gate (black dashed curve in fig 4a), the effect of the In₂O₃ gate on the Q factor is negligible. We should point out that the current moderate Q factor of our device is majorly limited by our fabrication errors. With optimized process, higher Q factor and lower insertion loss should be achievable. [22] As we apply the bias voltage on the In₂O₃ gate, electrons and holes start to accumulate at the In₂O₃/HfO₂ and Si/HfO₂ interfaces, respectively. The accumulated carriers induce modulation to both the real part and the imaginary part of the optical permittivity, and both contributes to the E-O modulation. The real part variation of the permittivity causes the resonance peak blue shift to shorter wavelength. By increasing the applied voltage from 0 to -4V, the resonant peak blue shifts by 1 nm, which corresponds to resonance tuning of 250 pm/V. It is among one of the largest tuning efficiencies induced by fast carrier effect (depletion and accumulation) ever reported so far. To have an easy comparison with conventional silicon MZI modulator, such tuning

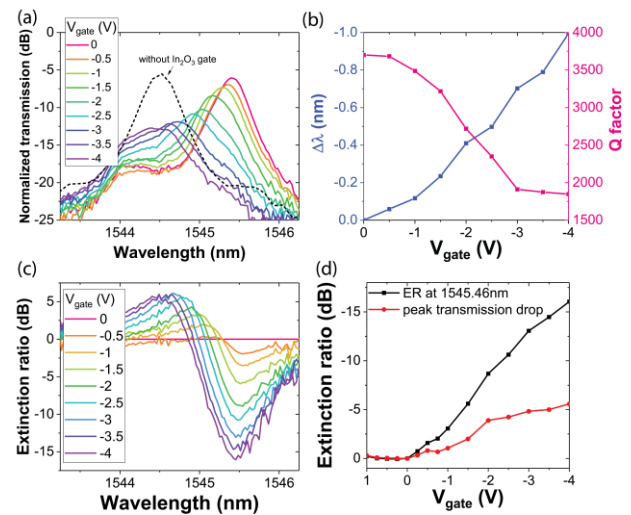


Fig 4. (a) Transmission spectra of the nanocavity modulator at different bias voltages (solid lines) and before sputtering the In₂O₃ gate (black dashed line). (b) Peak wavelength shift and Q factor as a function of applied bias. (c) Extinction ratio spectra at different bias voltages. (d) Extinction ratio at maximum efficiency wavelength (1545.46nm) and the peak transmission reduction as a function of the applied voltage.

efficiency corresponds to an equivalent $V_{\pi}L$ of 0.18 V·cm. Although higher tuning efficiency can be achieved through heavy carrier injection in PIN diode structures [23, 24], those devices suffer from the high energy consumption and low E-O modulation speed due to the life time of free carriers, which are not suitable for high speed modulators. The Q factor drops to 1,850 due to increased imaginary part of the permittivity as the voltage increases. The shift of the peak wavelength and the degradation of the Q factor are plotted in fig 4b. The imaginary part modulation of the optical permittivity, majorly from the In_2O_3 layer, also increases the optical loss and reduces the peak transmission.

Fig 4 (c) plots the extinction ratio (ER) spectra as a function of the applied bias. The maximum modulation is observed at 1545.46nm. The ER at this wavelength as a function of the applied voltage is shown in fig 4 (d). The flat band voltage of roughly 0V is observed, which is due to the similar Fermi levels of In_2O_3 and p-type silicon. An ER of 16dB is achieved with a bias changing from 0V to -4V. We also plot the peak transmission versus the applied voltage as shown in Fig 4 (d). With -4V applied voltage, the peak transmission drops by 5.6 dB. Compared with the peak transmission drop, the imaginary part modulation of the optical permittivity roughly contributes to around 1/3 to the total ER. The leakage current of the device at -4V is around 10^{-14} A, which is at the noise level of our measurement equipment. This also means the static power consumption of the MOS capacitor is negligible. The driving voltage for 3dB ER is reduced to less than 1V, 12 times less than our previous work, which is compatible with CMOS driving circuits. We can estimate the energy consumption of the modulator by $(CV^2/4)$ to be 3 fJ/bit. The driving voltage can be further reduced by decreasing the gate oxide layer thickness. For example, by decreasing the HfO_2 thickness to 5 nm, we can double the tuning efficiency to 500 pm/V, while decrease the driving voltage to 0.5V. If we can increase the Q factor to 5000, we can further decrease the driving voltage to 0.37V, achieving an energy efficiency of 0.8 fJ/bit.

The speed of the photonic crystal nanocavity modulator is only limited by the RC time constant given the moderate Q factor below 5,000. Considering the silicon doping level of our fabricated device, $\sim 10^{17}$ cm^{-3} , simulation shows a series resistance of $\sim 1\text{M}\Omega$, which yields a RC-delay limited speed of 0.12 GHz together with a capacitance of 13fF. In the AC measurement of the nanocavity modulator, the rising time of the transmitted optical signal shows a good match with our simulation analysis of $\sim 10^{-9}$ s. Unfortunately, a large falling time of $\sim 10^{-6}$ s is observed possibly due to the Schottky contact at the $\text{In}_2\text{O}_3/\text{Au}$ interface. We will address this challenge according to the suggestion from ref [12]. The RF bandwidth can be increased to 2GHz by simply increasing the silicon doping concentration to 5×10^{18} cm^{-3} . According to 3-D FDTD simulation [14], such doping concentration won't limit the Q factor up to at least 5,000. The additional insertion loss from increased doping level can be estimated by the passive waveguide loss (0.017dB/ μm for 5×10^{18} cm^{-3} doping concentration [14]) and the photon life time of the nanocavity ($\sim 4\text{ps}$ for Q factor of 5,000), which equals to only $\sim 1\text{dB}$. To further improve the performance, slab photonic crystal cavity design and advanced doping technique [23] must be used. Then, the series resistance can be reduced to less than 1 k Ω and the modulation bandwidth can be increased to over 12 GHz. High speed RF modulation will be implemented in our future design and characterization.

4. CONCLUSION

In summary, we demonstrate a low-voltage silicon photonic crystal nanocavity modulator with an ultra-short In_2O_3 electrical gate of only 350 nm in length, showing a large resonance tuning efficiency of 250 pm/V and an average modulation strength of 4dB/V for a medium Q factor of 3,700. One-volt CMOS compatible driving voltage is required to drive the 13 fF gate to achieve 3dB modulation, which corresponds to an energy efficiency of 3 fJ/bit. The performance of the device can be further improved to less than 0.5V operating voltage and sub-1fJ/bit energy consumption, offering the possibility to be directly driven by CMOS logic gates. These combined merits prove the great potential of the TCO-gated silicon nanocavity modulator for future CMOS driven integrated photonic interconnect systems.

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