

# Low-loss Subwavelength Grating Waveguide Bends Based on Index Engineering

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**Abstract:** We report the design, simulation and experimental demonstration of low loss subwavelength grating waveguide (SWG) bends. With trapezoidal shape silicon pillars, the average insertion loss of a 5 $\mu\text{m}$  SWG waveguide bend is reduced drastically from 5.43 dB to 1.10 dB per 90° bend for quasi-TE polarization.

**OCIS codes:** (050.6624) Subwavelength structures; (130.3120) Integrated optics devices

Silicon photonics has been attracting intensive interests in the last decade [1] due to its great potential in realizing low cost photonic chips with the readily-available CMOS manufacture technology [2]. However, the fact that silicon does not have either a direct band gap or the second-order nonlinearity makes it a great challenge to generate or control photons. Hybrid integration of silicon and functional cladding material has been considered as a potential solution to this issue [3]. Recently, subwavelength grating (SWG) waveguides, comprising of a periodic arrangement of high and low refractive index materials with a pitch less than one wavelength, have been demonstrated as a promising approach for the hybrid integration [4,5]. However, the practical applications of SWG waveguide have been greatly compromised by the large loss of SWG waveguide bends. For instance, a 10  $\mu\text{m}$  radius 90° bend has an insertion loss of ~1.5dB [5]. Therefore, to achieve the goal of building integrated photonics system with entirely SWG waveguides, it is extremely critical to investigate an innovative SWG waveguide bend with low-loss and small radius. In this paper, we propose an index engineering approach based on trapezoidal silicon pillars. This approach can effectively decrease the mode mismatch and radiation loss simultaneously, and thus can significantly reduce the bend loss.

A 3D schematic of a typical SWG waveguide is shown in Fig. 1(a), where  $A$  is the period of the SWG structure,  $l$ ,  $w$ , and  $h$  are the length, width, and height of silicon pillars, respectively. In our simulations and experiments, SU-8 ( $n=1.58$ ) is selected as the top cladding material. The period  $A$  is 300 nm. A typical silicon pillar (duty cycle equals to 0.5) has a geometry of  $l \times w \times h = 150 \text{ nm} \times 500 \text{ nm} \times 250 \text{ nm}$ . A 3D schematic of SWG bend built with rectangular silicon pillars is shown in Fig. 1(b) while SWG bend built with trapezoidal silicon pillars is shown in Fig. 1(c). We used full 3D FDTD simulation (FullWAVE<sup>TM</sup>, Synopsys Inc.) to scan parameters of the top and bottom bases of the trapezoidal silicon pillars to minimize the bend loss. The simulation results are summarized in a contour plot as shown in Fig. 2(a). It is found that a trapezoidal silicon pillar with 140 nm top base and 210 nm bottom base has the minimized bend loss of 0.192 dB per 90° bend, which is 50.1% of the bend loss (0.383 dB per 90° bend) of a conventional rectangular silicon pillar. The optical field profiles (Re[Hy] component) of 90° SWG waveguide bends of 5  $\mu\text{m}$  bend radius built with rectangular and trapezoidal silicon pillars are shown in Fig. 2(b) and (c), respectively. With the optimized design of silicon pillars, the optical field is better confined in the waveguide region (Fig. 2(b)) compared to the conventional SWG waveguide with rectangular pillars (Fig. 2(c)).

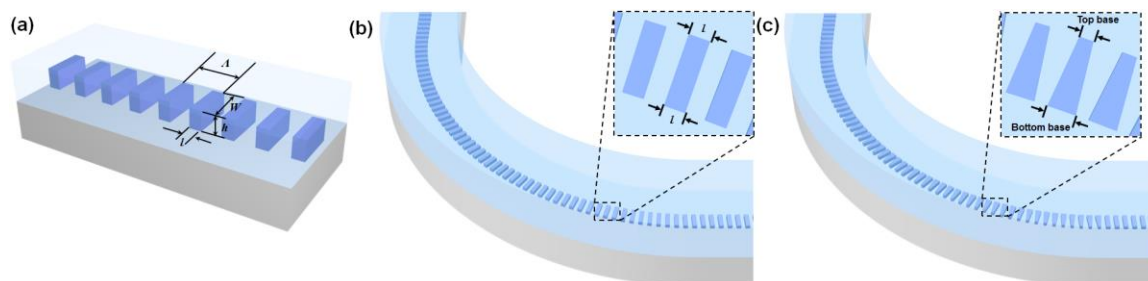


Fig.1 (a) 3D schematic of a SWG waveguide. (b) 3D schematic of SWG waveguide bend built with conventional rectangular silicon pillars. (c) 3D schematic of SWG waveguide bend built with trapezoidal silicon pillars.

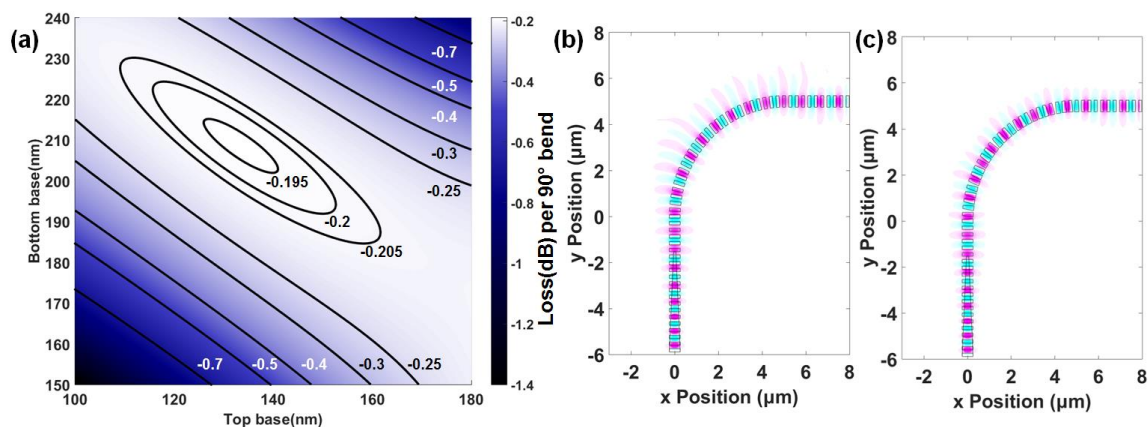


Fig.2 (a) Contour plot of bend loss for different top and bottom bases. Simulated field profiles of SWG waveguide bends built with (b) rectangular silicon pillars and (c) optimally tuned trapezoidal silicon pillars (140 nm top base and 210 nm bottom base)

Four types of silicon pillars: non-tuned rectangle (150 nm top base and 150 nm bottom base), under-tuned trapezoid (120 nm top base and 190 nm bottom base), over-tuned trapezoid (70 nm top base and 210 nm bottom base) and optimally-tuned trapezoid (140 nm top base and 210 nm bottom base) have been fabricated for demonstration. The devices are made on an SOI wafer (Soitec) with a 250 nm thick top silicon layer ( $n=3.476$ ) lying on a 3  $\mu\text{m}$  thick buried oxide (BOX,  $n=1.45$ ) layer. All structures are patterned in a single E-beam lithography (JEOL 6000 FSE) step. The patterns are then transferred into the silicon layer through reactive-ion-etching (PlasmaTherm 790). The agreement of the morphology of the devices with the design is confirmed by scanning electron microscopy (ZEISS Neon 40) as shown in Fig. 3(a)-(e). Fig. 3(f) shows the transmission spectra of the four representative bends between 1530nm and 1580 nm operating at the quasi-TE polarization. The insertion loss of the four representative bends at 1550nm is shown in Fig. 3(g), where the optimized trapezoidal silicon pillars is as low as 1.10 dB per 90° bend, only 20.3% of that of the non-tuned rectangular silicon pillars (5.43 dB per 90° bend).

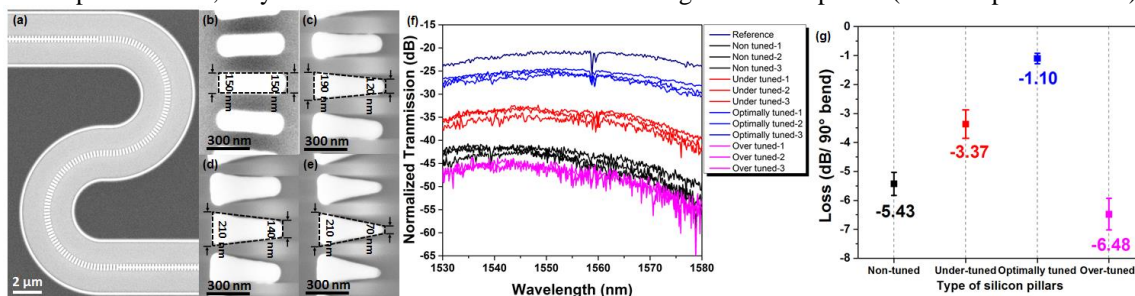


Fig. 3. (a) SEM image of a typical device. SEM images of (b) non-tuned silicon pillars, (c) under-tuned silicon pillars, (d) optimally tuned silicon pillars, and (e) over-tuned silicon pillars. (f) Transmission spectra of the four types of silicon pillars. (g) Statistical insertion loss of the four types of silicon pillars at 1550 nm.

In conclusion, we demonstrate the index engineering with trapezoidal silicon pillars can substantially reduce the insertion loss of SWG waveguide bends. Compared to SWG waveguide bends built with conventional rectangular silicon pillars, an average reduction of 79.7% of the insertion loss has been achieved experimentally. This study paves a road towards achieving all SWG waveguide based optical devices and circuits.

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