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Automated Logic Synthesis for Electro-optic Computing in Integrated Photonics

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ABSTRACT

As a tremendous amount of data is being created exponentially day by day, integrated optical computing starts to attract lots of attention recently due to the bottleneck in the continuation of Moore's law. With the rapid development of micro/nano-scale optical devices, integrated photonics has shown its potential to satisfy the demand of computation with an ultracompact size, ultrafast speed, and ultralow power consumption. As one of the paradigms in optical computing, the electro-optic logic that combines the merits of photonics and electronics has made considerable progress in various fundamental logic gates. It therefore becomes very critical to develop an automated design method to synthesize these logic devices for large-scale optical computing circuits. In this paper, we propose a new automated logic synthesis algorithm based on And-Inverter Graphs (AIGs) for electro-optic computing. A comprehensive component library of electro-optic logic is summarized with several new proposed logic gates. As an example, a large-scale ripple-carry full adder which serves as the core part of the arithmetic logical unit (ALU) is presented. In the design, all the electrical signals could be applied simultaneously at every clock cycle and then the light could process the signals through every bit at the speed of light without any delay accumulated. High-speed experiment demonstrations are carried out, which show its potential in future high-speed and low-power-consumption optical computing.

Keywords: Optical logic; integrated photonics; optical computing

1. INTRODUCTION

Moore's law states that the number of transistors on a chip doubles every two years or so while the costs are halved. It has continued for several decades and improved our society dramatically. However, recently, the doubling has started to falter because of the overwhelming heat generated when more and more transistors are squeezed into a chip[1]. In addition, when we are getting to 2-3 nm limit, electron behavior will be governed by quantum uncertainties which will make transistors unreliable. Therefore, researchers have done many investigations on various fields such as new materials, new fabrication technology, and new computing [2–7].

Optical computing is one of the most promising candidates that has attracted lots of interest in the past decade especially after the emergence of abundant mature integrated components, such as lasers, modulators[8–10] passive interconnects [11,12], and photodetectors[13]. It is a fact that electrical interconnect performance will dominate the total delay per gate in a 22 nm technology and below which results in a saturation of delay per gate of around 10 ps. As a comparison, it will be much faster for light to travel through an optical switch. For example, it only takes around 0.14 ps for light to go through a 10 um micro-resonator modulator that can be used as an AND gate[14]. That is one of the main advantages of optical computing. Researchers have done lots of both theoretical and experimental demonstrations of optical computing, from fundamental logic gates to complex optical computing circuits as well as high-level architecture[15–24].

Directed logic is one paradigm of optical computing architecture, which utilizes mature electrical circuits to set the states of each switch and then let light travel through the circuits to process the signals at every clock circle[25]. One important characteristic of direct logic is that the optical output of each gate will not be used as another control signals for another gate. It has two advantages. First, all optical gates that control light with light using nonlinear phenomena nowadays still consume lots of power and hard to be integrated compactly. As a result, this type of components is not suitable for power-

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efficient and compact computing circuits that are poised to beat the compact and powerful CMOS transistors. Second, using the output from the previous gate as the control signal of the next bit will result in a large latency since the delay will accumulate.

As lots of integrated optical components mature, electronic-photonic design automation (EPDA) has come onto the stage and become a hot topic just like the CMOS-based electronic design automation (EDA) several decades ago. EPDA will largely reduce the time consumption for designing as we are approaching large-scale computing circuits. Many big companies have started to jump into this area and release some prototype EPDA tools. The design flow includes specification, functional/logic design, circuit design[26], physical design, and physical verification. Some researches have been done on these aspects and various algorithms have been proposed.

In this paper, we will propose a new architecture of electro-optic logic (EOL) computing, which utilizes the advantages of electronics and photonics. Then we summarize all kinds of mature electro-optic logic gates and categorize them into three different groups. Traditional directed logic only uses one kind of gate, a 2x2 switch. Here we enlarge the library which could help reduce the circuit size and redundancy. Finally, an And-Inverter-graph based algorithm is proposed followed by several examples.

2. ARCHITECTURE

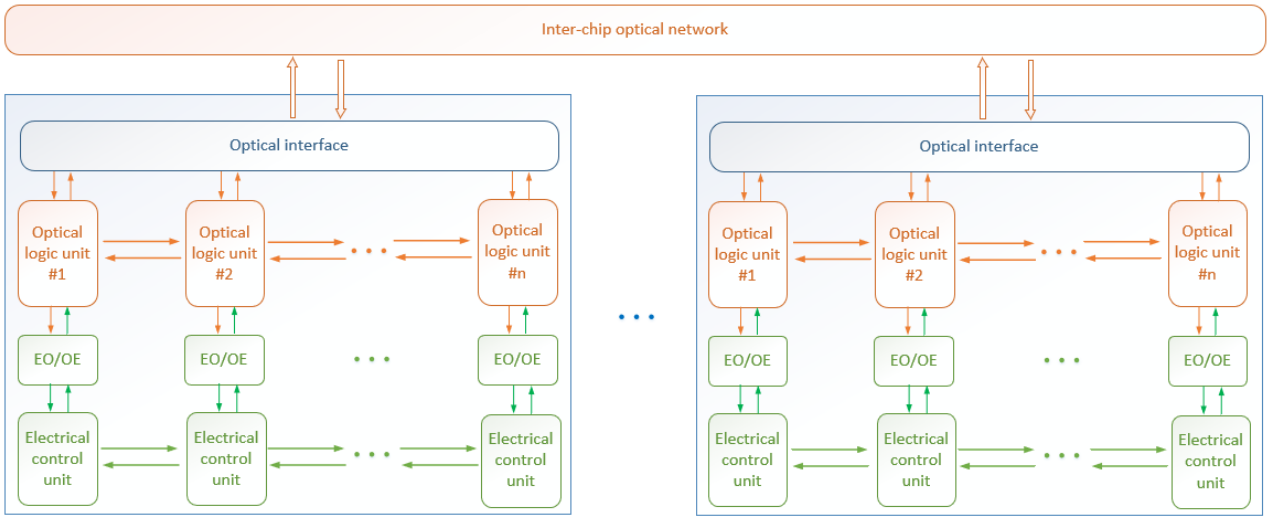


Figure 1. The architecture of the new proposed electro-optical logic computing

As the technology node goes to 22 nm and below, the performance improvement will be bottlenecked by the data transport. Because of this, interest has grown in high-bandwidth and low-power-consumption EOL computing. Figure 1 shows the architecture of the newly proposed EOL computing. The key part of the diagram is the optical logic unit, which contains various EOL gates. All these gates will be controlled by the electrical control units through the EO/OE modules. Electrical control units also include the memories since high-performance integrated optical memories are still not available. Then the optical logic units are capable of talking to its neighbors directly using light without OE/EO conversion. Compared to the electrical data transportation, optical methods could provide a much broader bandwidth, resulting in much faster computing speed. Even between different computing modules, the optical signals can travel through the inter-chip optical network directly such that the latency will be largely minimized.

3. BUILDING BLOCKS

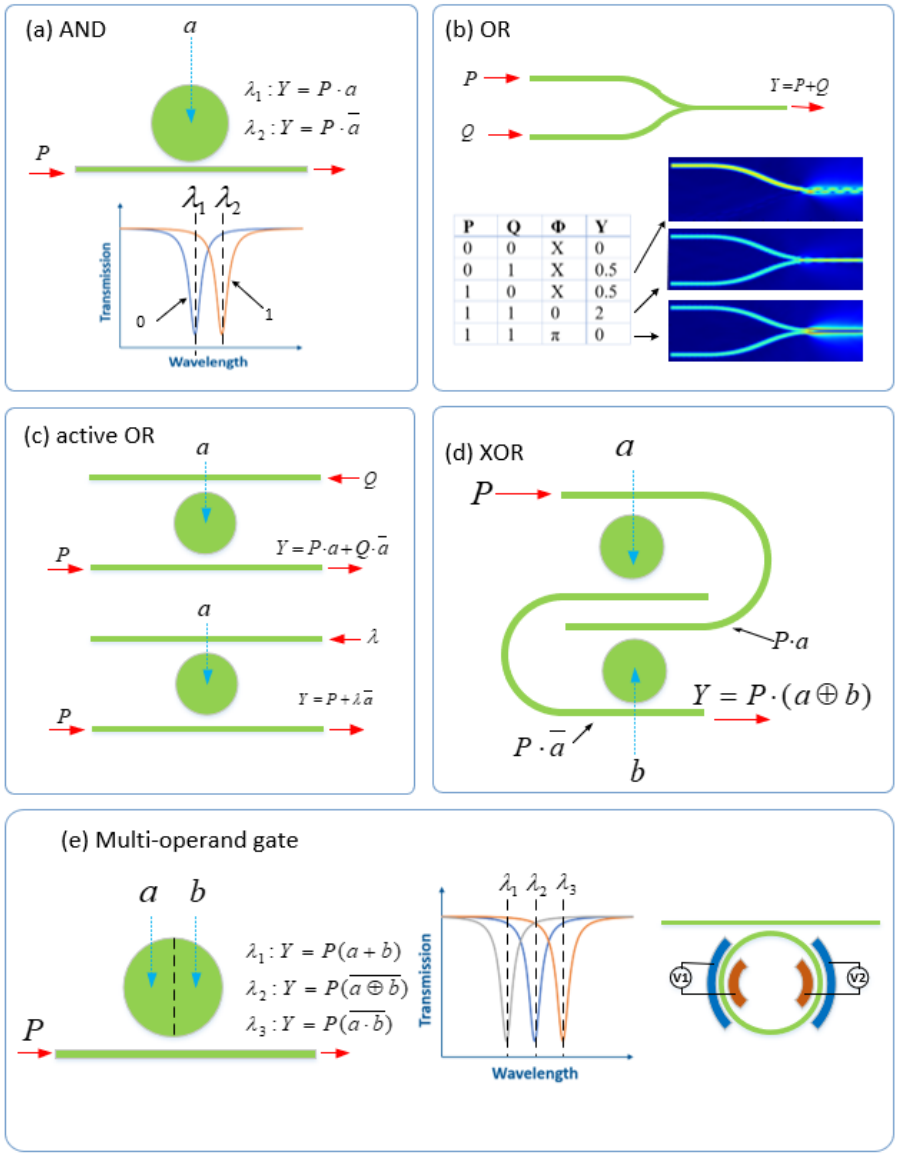


Figure 2. The schematics of (a) AND gates, (b) OR gates, (c)active OR gate, (d) XOR gate, (e) multiple-operand gates.[27]

Here we summarize the mature integrated and compact components that can be used as EOL gates for various functions. No matter in silicon platform or III-V platform, optical modulators have become one of the most fundamental active components that have a very stable performance to realize lots of different applications. Fortunately, a simple modulator alone could realize the function of AND, as shown in Figure 2(a). The figure shows a case for the resonator-based modulator, but it also fit for all other kinds of modulators such as electrical absorption modulator (EAM). Taking the resonator-based modulator as an example, we can see that when the electrical signal is applied into the modulator, the characteristic of the material will be changed and then the resonant spectrum will shift, which will finally switch the optical output. Whether the output logic is consistent with the electrical input or the opposite depends on the working wavelength. It should be noted that the result is the product of an optical signal and an electrical signal. The product of two optical signals is not feasible for now since low-power-consumption and compact all optical gate are still not available [28,29].

A combiner can be regarded as an OR gate at some circumstances. As shown in Figure 2(b), when there is only one arm of the combiner has light passing through, the optical output will be half of the input because of the mode mismatch and half of the light will be dissipated into the air out of the waveguide. When two arms both are lighted, the output will be a function versus the phase difference. If the phases are well controlled and matched, the results will be the sum of them. Therefore, a 3dB insertion loss is unavoidable, and the unevenness of the result will jeopardize the whole system especially at a cascaded circuit where the unevenness effect will accumulate along with the propagation path. There are two solutions to tackle with this issue. First, try to link the two independent inputs in order to cancel out the state of (1,1) which means two inputs are forbidden to be one simultaneously. The other way is to use active OR gate that is shown in Figure 2(c). It consists of a 2x2 modulator and the Q port should be set to be λ (continuous wave). With the electrical applied, the modulator will eventually choose one beam of light to go through, either the P or the Q. As a result, it eliminates the 3 dB loss. The output function will be $Y = P + \lambda \cdot \bar{a}$. This method can be implemented directly in a XOR gate, whose function is expressed as $Y = P \cdot (a \oplus b) = (P \cdot a) \cdot \bar{b} + (P \cdot \bar{a}) \cdot b$. According to this expression, it is easy to obtain the gate design as shown in figure 2(d).

Multi-operand modulators are being explored recently, which means one single modulator is controlled by multiple electrical inputs [30]. It is believed to have the potential to further increase the versatility and packing density of EOL computing circuit. For instance, figure 2(e) shows a microdisk modulator that are modulated by two signals, and the spectra are also shown in the inset. Based on the operating wavelength we set, the output function could be written as $Y = P(a + b)$, $Y = P\left(\overline{a \oplus b}\right)$, and $Y = P\left(\overline{a \cdot b}\right)$, respectively. Various logic circuits have been designed theoretically based on multi-operand modulators such as comparators, encoders, decoders, and adders[30].

4. AUTOMATED DESIGN ALGORITHM

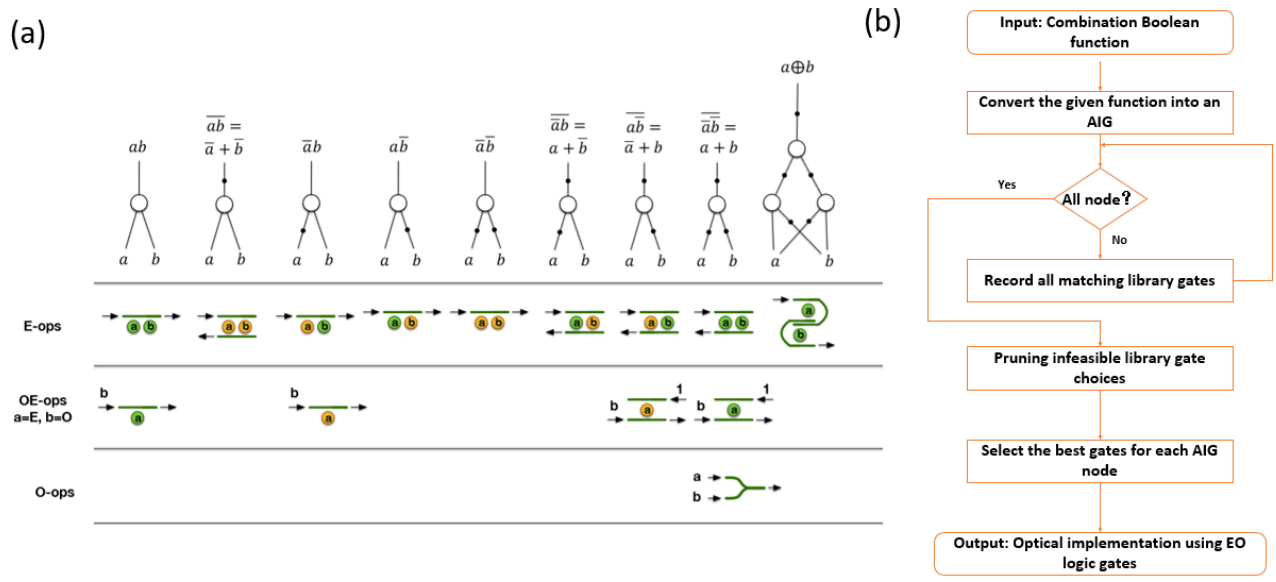


Figure 3. (a) Library of the EOL gates. (b) Flow chart of AIG algorithm.[27]

We categorize the fundamental EOL gates into three groups, E-ops, OE-ops, and O-ops based on their interfaces. The first row represents the function of the gate. The circle means AND, and the black dot means NOT. The second row represents the gates that can operate two electrical signals. The third row contains the gates are capable of processing one electrical signal and one optical signal. Since it is difficult to handle two optical signals without nonlinear effect, there are not many gates expect OR gate that we can collect into the library as listed in the last row.

The flow chart of the AIG based automated design algorithm is shown in Figure 3(b). AIG is a widely used algorithm in traditional EDA field [31]. It will convert any function into a graph consisting of AND and OR gates efficiently. Based on the library and the AIG algorithm, we can devise automatic logic synthesis algorithm similar to traditional COMS design. The flow chart of a high-level algorithm is shown in Figure 3(b). Given a combination Boolean function, it will first convert the function into an AIG, which can be further optimized by AIG-rewriting/balancing techniques [16]. For each node, this algorithm will look for the library gates that implement the sub-AIG, so that the functionality rooted at this node is equivalent to the AIG representation of the library gate. To this end, traditional mapping algorithm can be adopted[32]. Finally, prune infeasible library gate choices and select the best gets for each AIG node. The whole process can be well illustrated in the example shown in Figure 4.

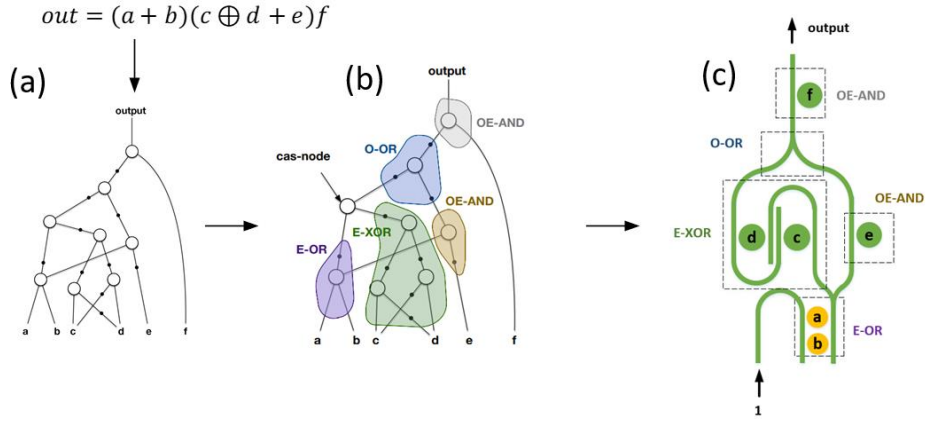


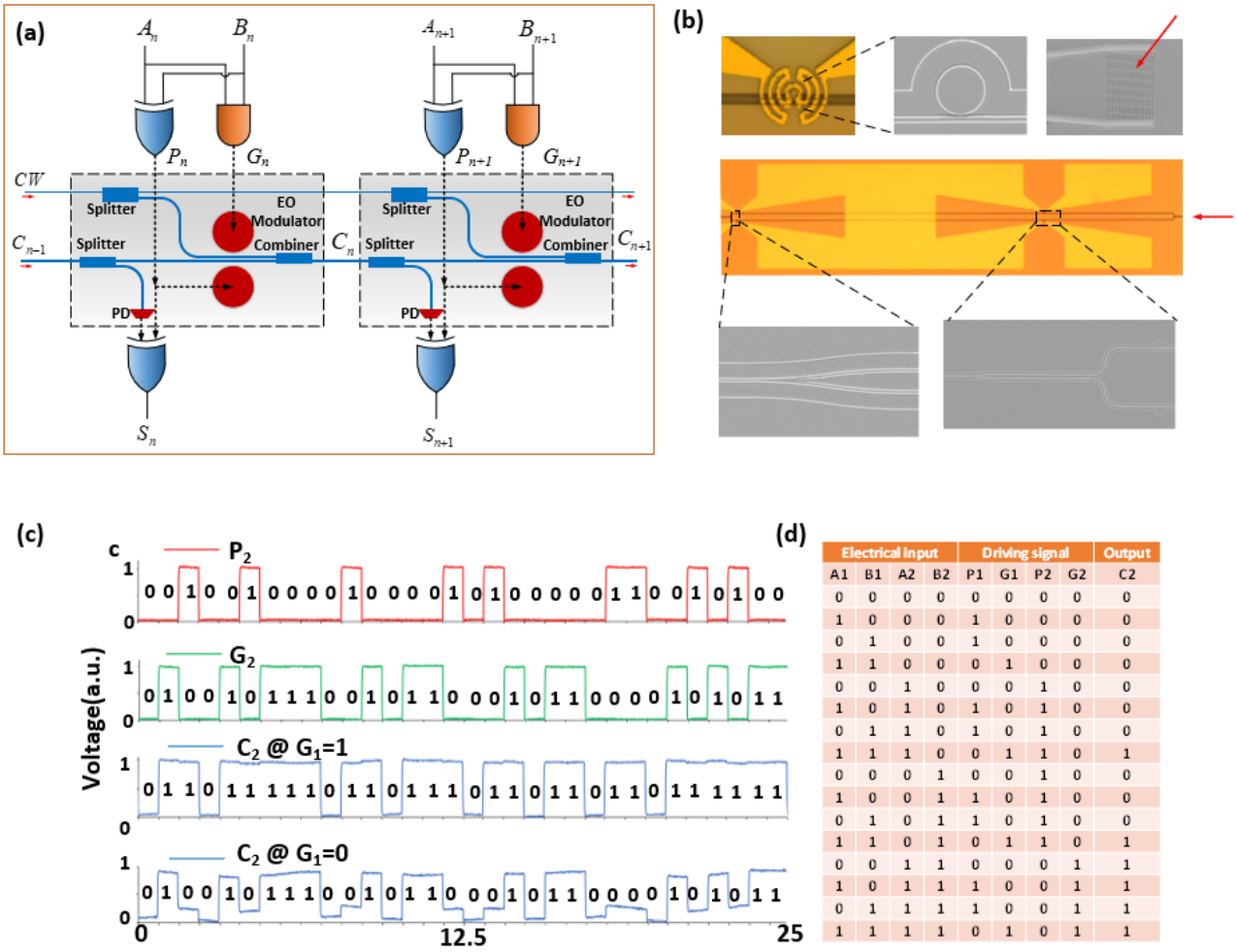
Figure 4. An example of the AIG-based design algorithm.[27]

The AIG-based algorithm has the ability to generate lots of EOL computing circuits automatically and efficiently without much redundancy. An auto-generated design of an EO full adder is shown in Figure 5(a). The expression of the inputs and outputs of a full adder can be written as

$$C_n = (A_n \oplus B_n) \cdot C_{n-1} + A_n \cdot B_n = P_n \cdot C_{n-1} + G_n \quad (1)$$

$$S_n = C_n \oplus (A_n \oplus B_n) = C_n \oplus P_n \quad (2)$$

where $P = A_n \oplus B_n$ (propagate) and $G_n = A_n \cdot B_n$ (generate). Now the components along the critical path are all replaced by optical components such as splitters, combiners, EO modulators, and photodetectors. Since light travels much faster than electronics on chip, the latency will be largely reduced for the whole circuit. A two-bit thermal-optic demonstration is carried out and microscope figures of the fabricated structure are shown in Figure 5(b). The EO modulator we chose here is the microdisk modulator with a radius of 2.5 μm. The analysis of the performance of the microdisk modulators is shown in[33]. Figure 5(c) shows the testing results of the two-bit full adder operating at 2.56kb/s, which is consistent with the truth table listed in (d).



Electrical input				Driving signal				Output
A1	B1	A2	B2	P1	G1	P2	G2	C2
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0	0
1	1	0	0	0	1	0	0	0
0	0	1	0	0	0	1	0	0
1	0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0	0
1	1	1	0	0	1	1	0	1
0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	0	0
0	1	0	1	1	0	1	0	0
1	1	0	1	0	1	1	0	1
0	0	1	1	0	0	0	1	1
1	0	1	1	1	0	0	1	1
0	1	1	1	1	0	0	1	1
1	1	1	1	0	1	0	1	1

Figure 5. EO full adder. (a) The schematic EO full adder. (b) The microscope figures of the fabricated full adder. (c) Experimental results. (d) Truth table. [20,34]

5. CONCLUSION

As integrated photonics develops with more integrated optical devices available, it becomes very imperative to develop an automated design method to synthesize these logic devices for large-scale optical computing circuits. In this paper, we propose an And-Inverter Graphs (AIG) based logic synthesis algorithm to design optical computing circuits automatically. Several examples are presented including a scalable ripple-carry full adder. Experiment demonstrations show the feasibility of this design as well as the advantages over electrical counterparts. This study paves the way for future high-speed and low-power consumption optical computing.

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