This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

High-Speed Plasmonic-Silicon Modulator Driven by Epsilon-near-zero Conductive Oxide

Bokun Zhou, Erwen Li, Yunfei Bo, and Alan X. Wang*

Abstract—**Transparent conductive oxides (TCOs) such as indium-tin oxide (ITO) have attracted increasing interests in integrated photonics and silicon photonics, owing to their large plasma dispersion and epsilon-near-zero (ENZ) effect. The nonlinear change of refractive index induced by free carrier modulation leads to a large electro-optic modulation with ultra-compact device footprint and unprecedented energy efficiency. However, high-speed modulation result is rare, mainly due to the lack of high-speed device design and fabrication quality. In this article, we characterize the fundamental electro-optic modulation structure consisting of Au/ITO/oxide/p-Si capacitor, showing that the property of ITO is greatly affected by the process condition. We also report an 8-µm-long hybrid plasmonic-silicon modulator driven by an ENZ ITO capacitor, achieving 100fJ/bit energy efficiency, 3.5 GHz modulation bandwidth and 4.5 Gb/s data rate. The electro-absorption modulator covers a broad optical bandwidth from 1515 to 1580 nm wavelength. For future development of such modulators, we point out that by replacing ITO with higher mobility TCO materials, we can achieve 40 GHz modulation bandwidth and 0.4 fJ/bit energy efficiency using a 3-µm-long device.**

Index Terms—**Electro absorption modulator, epsilon-near-zero material, plasmonic modulator, silicon photonics, transparent conductive oxide.**

I. INTRODUCTION

Plasmonics opens a new realm for ultra-compact, high-speed, and energy-efficient photonic devices that can transform next generation on-chip optical interconnect systems [1]–[3], owning to its ultra-strong optical confinement even below the diffraction limit [4]. Since traditional plasmonic materials such as gold and silver cannot provide the necessary electro-optic effect for active control of light and suffer high optical loss, various hybrid plasmonic-silicon photonic devices have been reported through the integration with active materials such as graphene [5], [6], electro-optic polymer[7], [8], and phase change materials [9]. Such hybrid plasmonic-silicon photonic devices take advantages of the matured silicon photonics platform for easy coupling, low optical loss and large-scale integration. In the meanwhile, they can achieve higher electro-optic modulation speed and higher energy efficiency than conventional silicon photonic devices by exploiting the strong Pockels effect [10]–[13] or the plasma dispersion effect [14], [15] of the integrated active materials.

In recent years, transparent conductive oxides (TCOs), such as indium-tin oxide (ITO), indium oxide (In_2O_3) and cadmium oxide (CdO), have attracted increasing interests owing to the large plasma dispersion effect and epsilon-near-zero (ENZ) effect[16]–[18]. Due to the dramatic change of free carrier concentration, TCOs can be electrically tuned from dielectric-like to metallic. During such transition, the absolute permittivity will reach a minimum value with real part crosses zero, which is described as the ENZ effect[19]–[21]. When ENZ occurs, light will be strongly confined in the ENZ layer due to the continuity of electric displacement normal to the interface, inducing strong electro-absorption (EA) of light over a broad optical bandwidth. To date, TCO-based EA modulators, such as plasMOStor [22] and plasmonic metal-oxide-semiconductor (MOS) waveguide modulator [23]-[24] have been demonstrated to achieve both large optical bandwidth and small device footprint, showing great potential for future integrated optical interconnect systems. However, only a moderate [25] digital modulation rate of 2.5 Gb/s was reported due to the large capacitance of the metal-oxide-semiconductor (MOS) capacitor and potential challenges of depositing high quality TCO materials.

In this work, we first characterize various Au/ITO/oxide/Si MOS capacitors, showing that TCO process conditions, such as low temperature baking and O_2 plasma treatment, can greatly affect properties of these MOS capacitors. Next, we design and demonstrate a hybrid plasmonic-silicon modulator driven by ITO. Through optimizing the device layout and adjusting the gate layer thickness, the capacitance is reduced to 100 fF while the series resistance remains small at 500Ω. The 8-µm-long EA modulator reaches 3.2 dB extinction ratio (ER) with only 2V voltage swing and 100 fJ/bit energy efficiency. More importantly, it achieves a high modulation bandwidth of 3.5 GHz and digital modulation rates to 4.5 Gb/s. To further improve the device performance, we prove through numerical simulation by integrating higher mobility TCOs. A 3-µm-long device can achieve a record-breaking performance with extremely small voltage swing of 0.2V, unprecedented energy efficiency of 0.4 fJ/bit, and a high modulation bandwidth of 40 GHz.

This work is supported by the AFOSR MURI project FA9550-17-1-0071 and NSF GOALI grant 1927271.

The authors are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: zhoubok@oregonstate.edu; lie@oregonstate.edu; boyu@oregonstate.edu; *wang@eecs.oregonstate.edu).

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

II. Characterization of Au/ITO/oxide/p-Si MOS capacitor

We first fabricated and characterized the fundamental electro-optic modulation structure of the EA modulator consisting of Au/ITO/oxide/p-Si MOS capacitor. The layered structure of the MOS capacitor is shown in Fig. 1 (a). 10 nm of SiO_2 gate oxide is thermally oxidized from the bottom p-Si. On top of that is the 15 nm ITO/Au gate. The electrical properties of ITO depend on the deposition and post-processing conditions [26]. The free carrier concentration can be tuned within the range of 1×10^{19} to 1×10^{21} cm^{-3} by controlling the oxygen/argon ratio of the gas flow during the RF sputtering, whereas the mobility is in the range of 15 to 25 $cm^2V^{-1}s^{-1}$, which are cross-checked using ellipsometry and Hall measurement. After the deposition, post annealing further increases the conductivity of ITO due to increase of mobility caused by crystallization, which has been systematically studied [27]. In addition, the ITO conductivity can also be increased by O_2 plasma treatment due to the injection of oxygen vacancies at the ITO surface[28]. This effect is especially significant for thin ITO films. For example, the carrier concentration of a 15 nm thick ITO film can be increased from 8×10^{19} to 4×10^{20} cm^{-3} by five-minute O_2 plasma treatment at 200 mTorr pressure. To be mentioned, the effect of O_2 plasma is reversible to some extent. The carrier concentration can be reduced from 4×10^{20} to 1×10^{20} cm^{-3} by 5 minutes of 180°C low temperature baking in air, which is common for some lithography process due to the reabsorption of oxygen in air.

We also compared MOS capacitors with two different ITO layers: high conductivity ITO (green dot, observed after O_2 plasma) and low conductivity ITO (red triangle, observed after low temperature baking). Fig. 1(b) plots the leakage current density at different gate voltages. The leakage current density of high-conductivity ITO capacitor shows a good match with the theoretical calculation based on Fowler-Nordheim tunneling [29]. Fig. 1(c) shows the AC capacitance density as a function of frequency at 5V bias voltage. The capacitance density of high conductivity ITO at low frequency matches the static capacitance density of 5×10^{-7} F/cm^2, which was simulated by Silvaco™ using the quantum moment model [30]. At higher frequency, the measured capacitance density is limited by the RC delay, which is calculated to be around 1 MHz due to the large capacitor area and high Si resistance. However, dramatic difference is observed for low-conductivity ITO. The leakage current density of low conductivity ITO capacitor is one order of magnitude smaller. Even at low frequency, the capacitance density is already more than one order of magnitude smaller than the static value. The capacitance density keeps decreasing as the frequency increases until reaching a flat region at which the capacitance is 3 orders of magnitude smaller than the static value at ~10^4 Hz. Such frequency response cannot be simply explained by the RC delay, indicating the existence of carrier transport processes for low conductivity ITO, which is not yet fully understood.

To conclude, the properties of TCO thin films highly depend on the process conditions, such as low temperature baking and O_2 plasma treatment. To minimize the effect from post-steps on ITO properties, we optimized the process flow in our fabrication. For high conductivity TCO-Si MOS capacitor, the performances match well with the theoretical calculation, the speed of which is only limited by the RC delay. However, for low conductivity TCO-Si MOS capacitor, both the leakage current and capacitance density suggest that there is more complex mechanism, which requires further investigation.

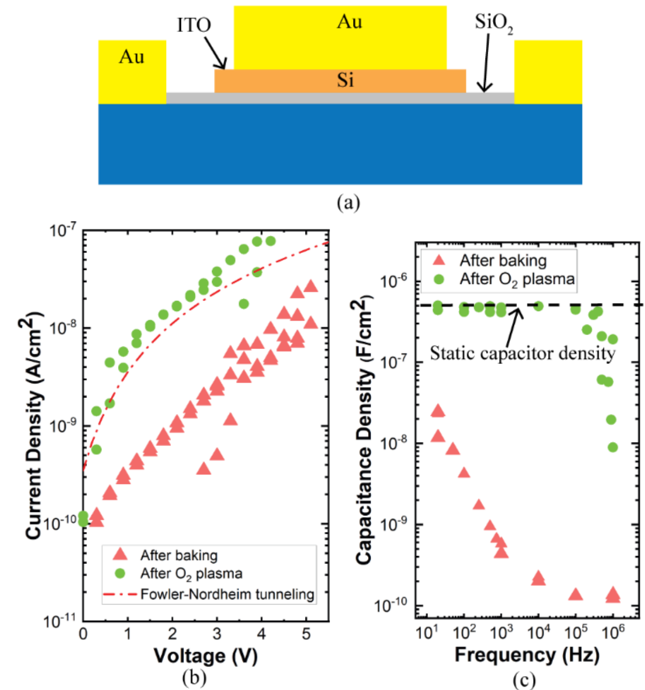


Fig. 1. (a) Cross sectional schematic of the Au/ITO/SiO_2/Si capacitor. (b) Leakage current density as a function of gate voltage for capacitors at different conditions. (c) Capacitance density as a function of frequency for capacitors at different conditions.

III. Design and Principle

The 3D schematic of the plasmonic ENZ EA modulator is shown in Fig. 2(a). The modulator is based on an Au/ITO/HfO_2/p-Si MOS capacitor in its active region. As illustrated in Fig. 2(b), the core of the p-type silicon rib waveguide is 250 nm in height and 450 nm in width, surrounded by 50 nm thick partially etched slab providing electrical conduction path. The waveguide is covered by 16 nm HfO_2 working as the gate insulator. On the top of that is the gate electrode consisting of 14 nm ITO and 100 nm Au film. Fig. 2(c) shows the device layout in the active region consisting of high-speed ground-signal-ground (GSG) electrodes, which will be discussed later.

We simulated the electro-absorption of the modulator. First, carrier distribution in the accumulation layer is simulated by Silvaco™ based on quantum moment model. The quantum moment model is proven to be more accurate in describing the carrier distribution of accumulation layer in a MOS capacitor with an ultra-thin insulator, which is critical to predict the onset of the ENZ field confinement. A thorough discussion can be found in ref. [30]. Next, the carrier distribution is imported into Lumerical MODE for finite difference eigenmode simulation. The optical properties of ITO and Si can be described by the well-established Drude model [31]:

$$\epsilon_r = \epsilon' + i\epsilon'' = \epsilon_\infty - \frac{\omega_p^2}{\omega^2+\gamma^2} + i\frac{\omega_p^2\gamma}{\omega(\omega^2+\gamma^2)} \quad (1)$$

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

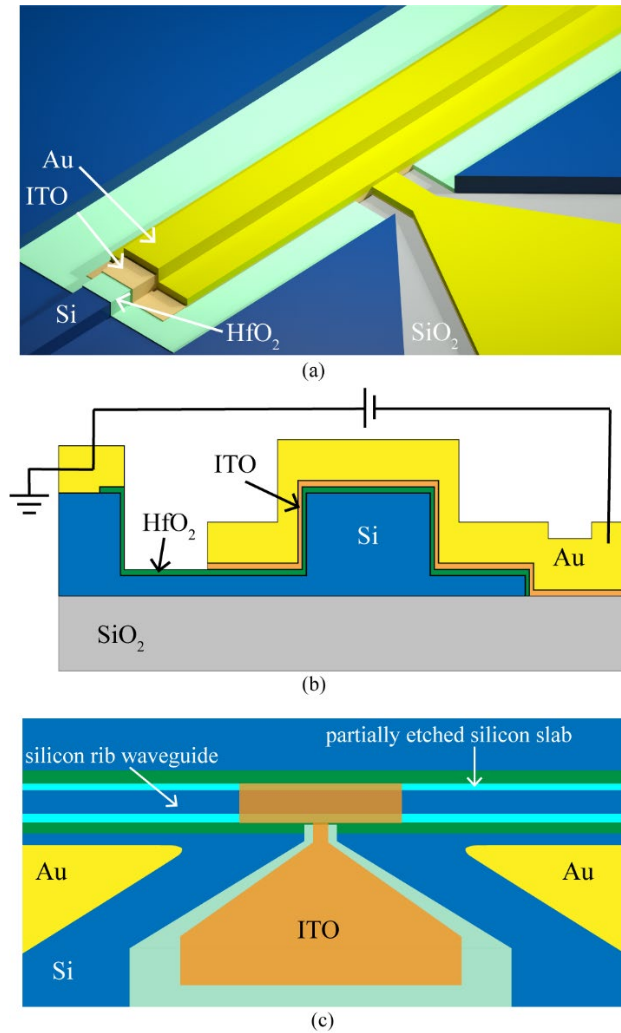


Fig. 2. (a) 3D schematic of the hybrid plasmonic-TCO-silicon EA modulator. (b) Cross sectional and (c) top view schematic of the EA modulator. Core waveguide is 450 nm in width and 250 nm in height, with slab of 50 nm in height.

Here, ϵ_∞ is the high-frequency dielectric constant. ω_p is the plasma frequency, which is proportional to the carrier concentration N_c by $\omega_p = \frac{N_c q^2}{\epsilon_0 m^*}$, where q is charge of electron. ϵ_0 is permittivity of vacuum and m^* is the effective mass of the carrier. The plasma collision frequency γ is inversely proportional to the carrier mobility μ by $\gamma = \frac{m^*}{q\mu}$. The change of carrier concentration results in the change of both real and imaginary part of the permittivity. Due to the small high-frequency dielectric constant and large carrier concentration, the real part permittivity of ITO can be reduced to zero and the absolute value of the permittivity reaches the minimum, which is the so-called ENZ state.

Fig. 3(a) shows the hybrid plasmonic-silicon waveguide mode profile of the transverse-electric (TE) mode at 0V bias, representing a low loss state (ON state). The mode profile is plotted in log scale to show the electric filed intensity both in the center and in the ITO layer. The propagation loss of the device is 1.6 dB/μm in simulation. Upon negative biasing the MOS capacitor, electrons and holes accumulate at the ITO/HfO_2 and Si/HfO_2 interface, respectively. The accumulation of free carriers induces light absorption. The changes of free carrier concentration distribution and refractive index distribution inside ITO layer are shown in Fig. 3(b). Normal to the HfO_2/ITO interface, the major change occurs within the 1nm-thick accumulation layer. Fig. 3(c) compares the zoomed-in mode profile at the waveguide side-interface at 0V and -8V bias. Under the same linear scale, it is clearly shown

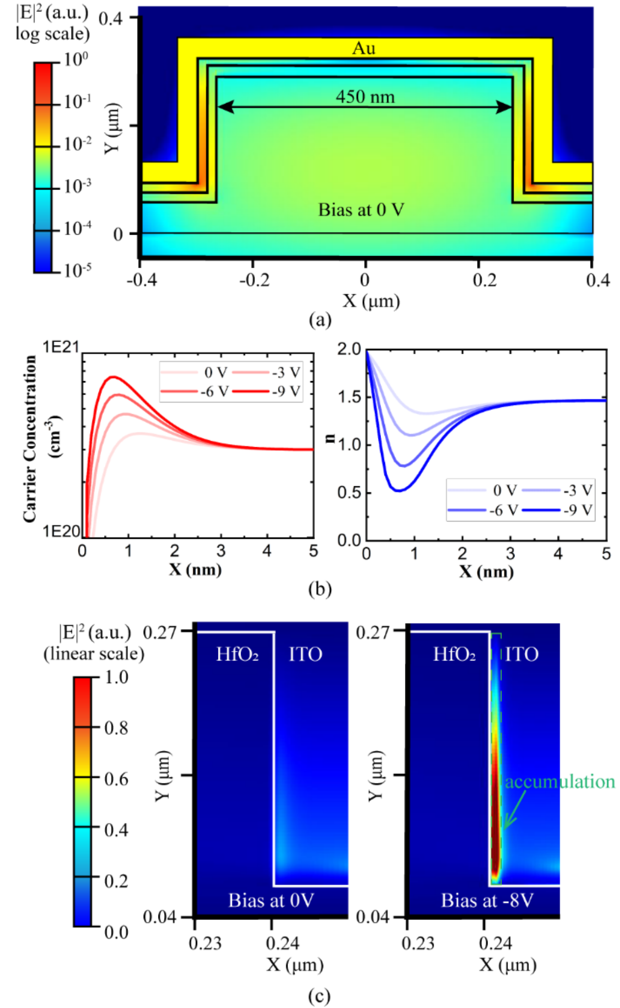


Fig. 3. (a) Simulated mode profile at 0V bias in the active region using Lumerical MODE. (b) Carrier concentration distribution and refractive index distribution in the ITO accumulation layer, normal to the HfO_2/ITO interface, as a function of applied bias from 0V to -9V. (c) Enlarged view at the HfO_2/ITO interface, showing field in accumulation layer at 0V and -8 V bias. Light is strongly confined in the 1 nm accumulation layer. (d) Simulated transmission and modulation strength for waveguide width of 450 nm

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

that at 0V bias, the electric field is relatively uniform in the ITO layer, whereas at -8V bias, the electric field is strongly confined in the accumulation layer at the HfO_2/ITO interface owning to the continuity of electric displacement. Fig. 3(d) plots the extinction ratio (ER) and modulation strength as a function of the applied bias. Clearly, there are two stages of operation. At small bias, the extinction ratio increases almost linearly versus the applied bias because the loss induced by free carrier absorption is proportional to the concentration of free carriers. At large bias, when the ITO accumulation layer reaches the ENZ state, the absorption is further enhanced due to the optical field confinement. The ER increases to 1.2 dB/µm at -8V bias. According to the carrier distribution simulation, the peak carrier concentration of the ITO accumulation layer reaches ENZ carrier concentration of 6.5×10^{20}cm^{-3} at -6.5V, indicating the onset of ENZ confinement. Theoretically, by biasing the modulator at the ENZ region, we can modulator the device with a much smaller voltage swing. From the simulation, the modulation strength peaks around -6.5V bias, reaching 0.28 dB/(V·µm). For example, this corresponds to a voltage swing of V_{pp}=1.4 V for 3-dB ER in an 8µm-long EA modulator.

The bandwidth of the hybrid plasmonic-silicon EA modulator is primarily limited by the RC delay, which can be estimated by $f=\frac{1}{2\pi RC}$, due to the accumulation mode operation. In order to achieve high speed operation, we improved our device design in two aspects compared with our previous demonstration [32]. First, the total capacitance is reduced by minimizing the gate electrode overlapping with the bottom silicon layer. Fig. 2(c) shows part of the device layout. Based on the capacitance density of 8 fF/µm^2 from the simulation, the total capacitance is around 100 fF. Second, because the ITO is covered by Au film, the series resistance mainly comes from the Si conduction path. To reduce the series resistance, the top 50 nm of the silicon layer is heavily doped to 1×10^{20} cm^{-3}. The series resistance can be reduced to <100Ω, which will give us a modulation bandwidth over 15GHz in design for 8µm-long EA modulator.

IV. Fabrication and Characterization

A. Fabrication Processes of the EA modulator

The hybrid plasmonic-silicon EA modulator is fabricated on a commercial silicon-on-insulator (SOI) wafer, with 250 nm silicon layer and 3 µm buried oxide. First, the slab waveguide and grating couplers are patterned by two-step electron-beam lithography (EBL) and reactive ion etching (RIE). At the top 50nm-thick silicon layer, the active region and contact regions are highly doped by ion implantation with 5 keV of B^+ ions at a flux of 6×10^{14} cm^{-2}, equivalent to a dopant concentration of 1×10^{20} cm^{-3}. After ion implantation, the dopants are activated by rapid thermal annealing (RTA) at 1000 °C for 10 s. Next, 16 nm-thick HfO_2 layer is conformably deposited using atomic layer deposition (ALD). After ALD, ITO/Au gate layer is patterned by EBL. Then, 14 nm of ITO and 100 nm of gold are RF sputtered [33] and thermally evaporated, respectively, followed by a lift-off process. The ITO is sputter at 1% O_2/Ar gas flow, yielding a carrier concentration of 3×10^{20} cm^{-3}. The HfO_2 gate oxide in the silicon contact region is removed using buffered hydrofluoric acid. After that, an Ni/Au coplanar GSG

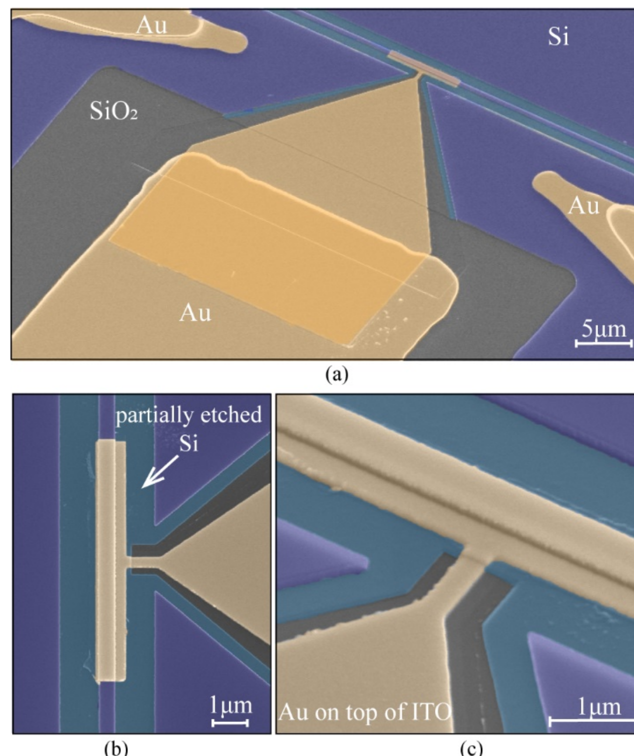


Fig. 4. (a) Scanning electron micrograph (SEM) of the fabricated 8-µm-long EA modulator with false color. Enlarged (b) top view and (c) tilted view of active region.

electrode is patterned by optical photolithography to form Ohmic contacts. The fabricated device is shown in Fig. 4(a). In Fig. 4(b), the zoomed-in view shows the active region of the EA modulator. The partially etched slab is shown in the tiled view in Fig. 4(c).

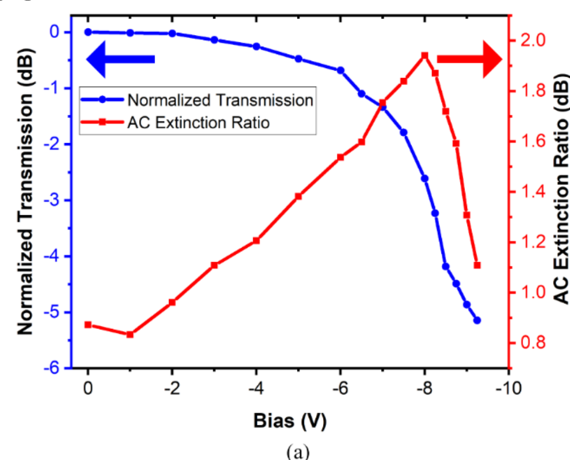
B. Testing of the Plasmonic ENZ EA modulator

To test the EA modulator, light is coupled into and out of the silicon waveguide through the waveguide grating couplers. The input/output fibers are mounted at a tilted angle of 10°. A polarization controller is used at the input side to excite TE mode. The insertion loss (IL) of the hybrid plasmonic-silicon waveguide is estimated to be 2.7 dB/µm, which can be calculated from fitting the optical loss of devices with different length. The measured IL is larger than the simulated value of 1.6 dB/µm. We articulate that there are two major reasons for the discrepancy. First, the material property in the simulation model differs from the actual thin film. For example, the permittivity of Au used in the simulation is based on ideal bulk material. As comparison, the thermally evaporated Au thin film in the experiment is known to be low-density with rough grain boundaries, which usually has three times larger imaginary part of the optical permittivity [34]. Similarly, the optical property of TCO is highly dependent on process condition. The non-ideality from the sputtering process such as non-uniformity, grain boundaries may all contribute to additional optical loss of the waveguide. Second, the waveguide surface roughness from EBL and RIE processes plays a critical role because the optical scattering loss can be significantly enhanced by the plasmonic effect [35]. The localized plasmonic mode bounded at the metal-dielectric interface can be strongly scattered by the waveguide surface roughness, even at a few nanometer scale.

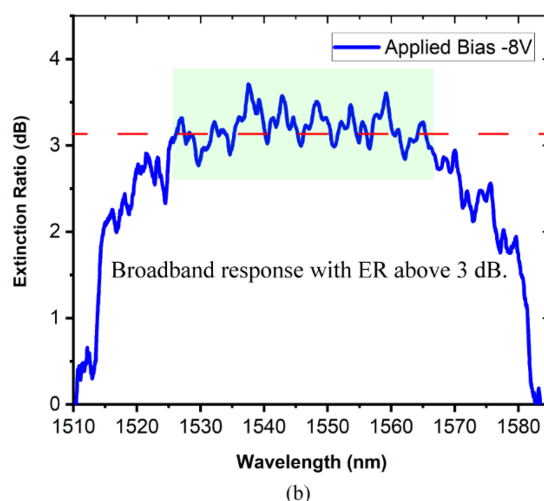
0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

A DC bias is applied across the capacitor. Fig. 5(a) shows the transmission at 1.55 μm of an 8-μm-long modulator at different DC biases (blue line) normalized to zero bias. The trend matches well with our simulation. A dramatic increase of absorption is observed at larger bias. From -6V to -8V, the transmitted power reduces by 3.2 dB, indicating that the ITO in accumulation layer has reached ENZ condition. The red line in Fig. 5(a) shows the AC modulation ER at different DC bias voltages, which is defined as difference of transmitted power at each bias with 1V voltage swing. It shows that at -8V bias, the AC ER is more than 2 times larger than that at 0V bias. In Fig. 5(b), the fabricated modulator exhibits a relatively uniform optical modulation bandwidth from 1515 to 1580 nm, which is mainly limited by the bandwidth of our grating couplers [36]. The intrinsic modulation bandwidth comes from the nature of ENZ effect. Shorter wavelength requires larger carrier concentration to trigger ENZ enhanced absorption. Our simulation indicates a short wavelength limit to 1.45 μm for the measured applied bias, which exceeds the bandwidth of the grating coupler. The fringes on the spectrum comes from the reflection between two grating couplers. The distance between two grating couplers L is 500 μm and the group index n_g is 2.64.The wavelength free spectral range (FSR) is calculated by $\Delta\lambda_{FSR} = \lambda^2/n_g L \approx 1.82\ nm$, which roughly matches with the fringe period.

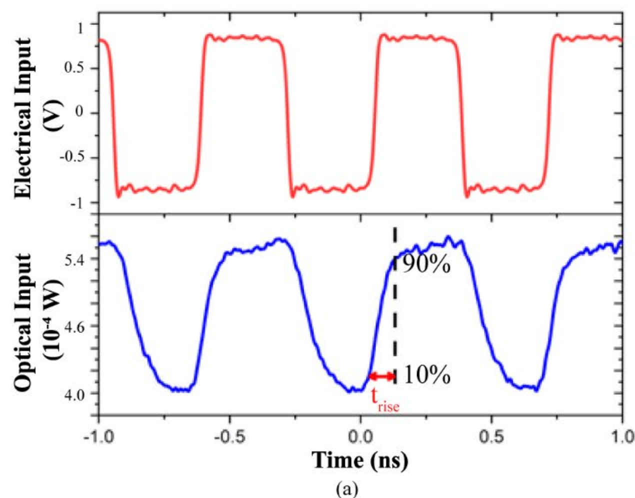


(a)

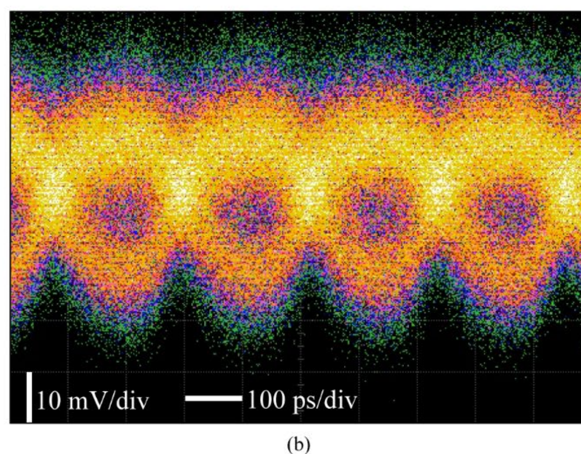


(b)

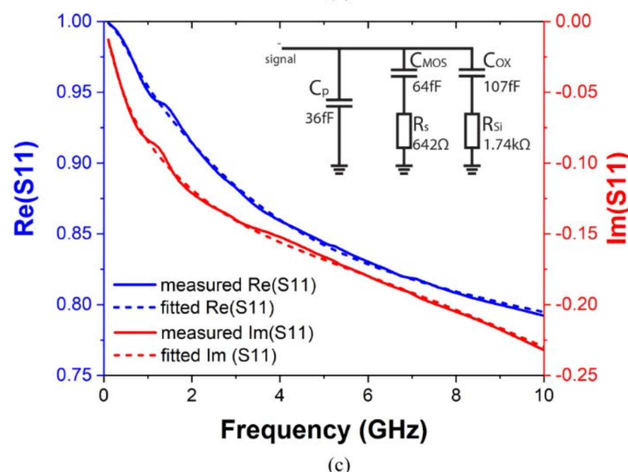
Fig. 5. (a) Experimental DC transmission and AC modulation strength for 8-μm-long device at different bias. (b) Extinction ratio at -8V bias, showing broadband response from 1515 nm to 1580 nm.



(a)



(b)



(c)

Fig. 6. (a) 1.5 GHz AC modulation of the fabricated device. (b) Eye diagram of 4.5 Gb/s digital modulation. (c) Real part and imaginary part of the measured and fitted S11 parameters. Inset: equivalent circuit model extracted from the S11 parameter fitting.

Fig. 6(a) plots the modulation waveform of the modulator at 1.5 GHz. The upper curve shows the electrical input of the device, whereas the lower curve is optical output to the Digital Communication Analyzer (DCA) oscilloscopes, showing electro-optical modulation. The rising time (10%-90%) is measured to be ~0.1ns, which gives a bandwidth of ~3.5 GHz. We measured and fitted the S11 parameters of the modulator as shown in Fig. 6(c). The inset of Fig. 6(c) illustrates the extracted equivalent circuit. Here, C_p is the parasitic capacitance between

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

contact pads, and C_{OX} and R_{Si} are the parasitic capacitance over the buried oxide layer and the corresponding resistance. The modulation speed is determined by the MOS capacitance C_{MOS} and the device series resistance R_s, which are fitted to be 64 fF and 642Ω. These two give us a RC bandwidth of 3.8GHz, which matches well with the measured modulation bandwidth. The MOS capacitance is slightly less than the designed value, which may be attributed to dimension errors of the device fabrication or the non-uniformity of the ITO film. However, the series resistance is more than 6× larger than the estimated value of 100 Ω in our design, which is the limiting factor to achieve the designed modulation bandwidth of 15 GHz for a 8-μm-long EA modulator. We measured the sheet resistance of heavily doped silicon slab to be ~1100 Ω/□, which larger than the design value of ~200 Ω/□. We anticipate that the large silicon resistance is mainly due to fabrication imperfection of the silicon implantation and the annealing condition, which can be further improved. Fig. 6(b) shows the eye diagram of 4.5 Gb/s data rate with $2V_{pp}$ voltage swing. The ON and OFF states can be clearly seen. Two main reasons are responsible for the limited open width of the eye diagram. First, the optical output to the DCA for eye diagram is close to the noise level of our instrument due to high device loss, which would be improved by optimizing taper design and fabrication process in the future work. Second, the interfacial states in the MOS structure would compromise the performance, which requires further investigation. The energy consumption is estimated to be 64 fJ/bit using $CV_{pp}^2/4$.

V. Future Design using High Mobility TCOs

The operation of the modulator replies on ENZ-induced field enhancement. The enhancement factor is inversely proportional to the absolute value of the permittivity, which approximately equals to the imaginary part of permittivity and inversely proportional to the carrier mobility of TCO, $|\varepsilon_{ENZ}| \approx \varepsilon''_{ENZ} \propto {\mu_{TCO}}^{-1}$. The larger the carrier mobility is, the smaller the permittivity is at the ENZ condition. Thus, the field enhancement of the plasmonic ENZ EA modulator can be further improved by high mobility TCO materials. It has been suggested that CdO with a high mobility of 300 $cm^2V^{-1}s^{-1}$ can potentially reach an ER over 5dB/μm [37]. But the dependence of driving voltage and energy efficiency on mobility is not clearly stated. Here, we simulated and compared the performance of hybrid plasmonic-silicon EA modulators using similar MOS capacitor structure with different TCOs. Table I lists TCOs with different carrier mobility and the corresponding absolute value of the ENZ permittivity. The results are shown in Fig. 7(a). As the mobility of TCO increases, two effects can be observed. First, the maximum ER is increased, which means shorter device length can be achieved. Second, the onset of the ENZ-enhanced plasma absorption becomes steeper, which means lower voltage swing is required. Table I also shows the simulated IL with the free carrier concentration of $3\times10^{20}cm^{-3}$, which clearly proves that high mobility TCOs also reduces the IL at the "ON" state.

TABLE I Permittivity |ε| at ENZ for TCOs of different mobility

TCO Materials	Mobility ($cm^2V^{-1}s^{-1}$)	ENZ |ε|	Effective Mass	Reference	Simulated IL (dB/μm)
ITO	15~30	0.96	0.33-0.35	[26], [28]	1.66
In_2O_3	20~35	0.42	0.3-0.32	[28], [38]	0.89
$Ti:In_2O_3$	70~100	0.15	0.27-0.31	[39]	0.64
CdO	280~300	0.05	0.22-0.24	[37]	0.46

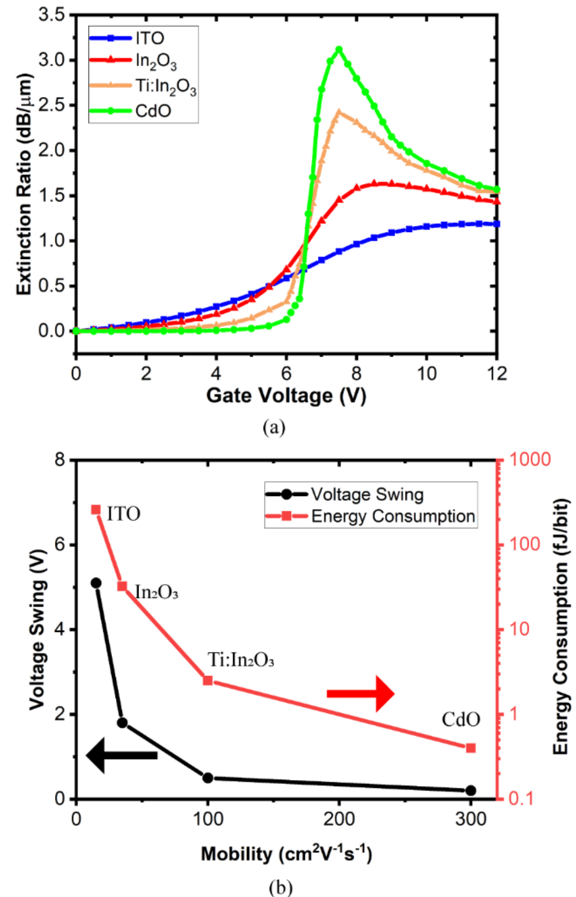


Fig. 7. (a) Comparison of extinction ratio for hybrid plasmonic-silicon EA modulators driven by different mobility TCOs. (b) Voltage swing required to achieve 1 dB/μm modulation strength for TCOs with different mobility and the corresponding energy efficiency.

Overall, we can make the plasmonic-silicon EA modulators more compact and energy efficient using high mobility TCOs. For example, to achieve a 3dB ER of a 3-μm-long ENZ modulator, the required voltage swing reduces from 5.1V to 0.5V with mobility increased from 15 $cm^2V^{-1}s^{-1}$ (ITO) to 100 $cm^2V^{-1}s^{-1}$ ($Ti:In_2O_3$), or to 0.2V with mobility increased to 300 $cm^2V^{-1}s^{-1}$ (CdO). Correspondingly, the energy consumption for a 3-μm long device reduces from 260 fJ/bit to 2.5 fJ/bit and 0.4 fJ/bit, calculated by $CV_{pp}^2/4$. To clarify, the resistance majorly comes from the conduction path from the electrode to the center of the active region through Si slab, which is a fixed distance in current design. The shorter device length would only reduce the capacitance to be around 40fF, providing the same capacitance density, while maintain the same resistance. With improved condition of doping and annealing, the resistivity of Si slab would reach the designed value of 1×10^{-3} Ω·cm, corresponding to series resistance less than 100Ω [25]. Moreover, the electrode could be put closer to the center of the active region, once the device length shortened. Correspondingly, high modulation bandwidth is estimated to be over 40 GHz, calculated by $f = \frac{1}{2\pi RC}$.

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2020.2979192, Journal of Lightwave Technology

VI. Conclusion

In summary, we characterized the fundamental electro-optic modulation structure consisting of Au/ITO/oxide/p-Si capacitor and showed that the property of ITO is greatly affected by the process condition. We reported an 8-μm-long plasmonic-TCO-silicon EA modulator with 3.5 GHz modulation bandwidth and broadband response from 1515 nm to 1580 nm. By biasing the device at the ENZ region, 3.2 dB ER with 2V voltage swing is observed. Eye diagram of 4.5 Gb/s digital modulation is measured. Furthermore, we demonstrated the dependence on TCO mobility for extinction ratio and energy consumption of EA modulator, based on enhanced ENZ effect. By adopting high mobility TCOs, a record-breaking device performance of energy consumption of 0.4 fJ/bits and high speed over 40 GHz is expected for a 3-μm-long EA modulator.

Acknowledgment

The authors would acknowledge the support from the EM Facility and MASC center at Oregon State University for the device fabrication.

References

[1] V. J. Sorger, R. F. Oulton, R. M. Ma, and X. Zhang, “Toward integrated plasmonic circuits,” *MRS Bull.*, vol. 37, no. 8, pp. 728–738, 2012.
[2] A. Emboras *et al.*, “Electrically controlled plasmonic switches and modulators,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 21, no. 4, 2015.
[3] S. A. Maier, “Plasmonics: The promise of highly integrated optical devices,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 12, no. 6, pp. 1671–1677, 2006.
[4] Ekmel Ozbay, “Plasmonics : Merging Photonics and Electronics at Nanoscale Dimensions,” *Science (80-.).*, vol. 189, no. 2006, pp. 189–194, 2012.
[5] N. Youngblood, Y. Anugrah, R. Ma, S. J. Koester, and M. Li, “Multifunctional graphene optical modulator and photodetector integrated on silicon waveguides,” *Nano Lett.*, vol. 14, no. 5, pp. 2741–2746, 2014.
[6] M. Liu *et al.*, “A graphene-based broadband optical modulator,” *Nature*, vol. 474, no. 7349, pp. 64–67, 2011.
[7] C. Y. Lin *et al.*, “Electro-optic polymer infiltrated silicon photonic crystal slot waveguide modulator with 23 dB slow light enhancement,” *Appl. Phys. Lett.*, vol. 97, no. 9, pp. 2008–2011, 2010.
[8] F. Ren *et al.*, “Surface-normal plasmonic modulator using sub-wavelength metal grating on electro-optic polymer thin film,” *Opt. Commun.*, vol. 352, pp. 116–120, 2015.
[9] P. Markov, K. Appavoo, R. F. Haglund, and S. M. Weiss, “Hybrid Si-VO_2-Au optical modulator based on near-field plasmonic coupling,” *Opt. Express*, vol. 23, no. 5, p. 6878, 2015.
[10] A. Melikyan *et al.*, “High-speed plasmonic phase modulators,” *Nat. Photonics*, vol. 8, no. 3, pp. 229–233, 2014.
[11] R. Ding *et al.*, “A low VπL modulator with GHz bandwidth based on an electro-optic polymer-clad silicon slot waveguide,” *IEEE Int. Conf. Gr. IV Photonics GFP*, vol. 18, no. 15, pp. 201–203, 2010.
[12] J.-M. Brosi, C. Koos, L. C. Andreani, M. Waldow, J. Leuthold, and W. Freude, “High-speed low-voltage electro-optic modulator with a polymer-infiltrated silicon photonic crystal waveguide,” *Opt. Express*, vol. 16, no. 6, p. 4177, 2008.
[13] L. Alloatti *et al.*, “42.7 Gbit/s electro-optic modulator in silicon technology,” vol. 19, no. 12, pp. 11841–11851, 2011.
[14] J. A. Dionne, K. Diest, L. A. Sweatlock, and H. A. Atwater, “PlasMOStor: A metal-oxide-si field effect plasmonic modulator,” *Nano Lett.*, vol. 9, no. 2, pp. 897–902, 2009.
[15] V. J. Sorger, N. D. Lanzillotti-Kimura, R. M. Ma, and X. Zhang, “Ultra-compact silicon nanophotonic modulator with broadband response,” *Nanophotonics*, vol. 1, no. 1, pp. 17–22, 2012.
[16] E. Li, Q. Gao, S. Liverman, and A. X. Wang, “One-volt silicon photonic crystal nanocavity modulator with indium oxide gate,” *Opt. Lett.*, vol. 43, no. 18, pp. 4229–4432, 2018.
[17] E. Li, Q. Gao, R. T. Chen, and A. X. Wang, “Ultracompact Silicon-Conductive Oxide Nanocavity Modulator with 0.02 Lambda-Cubic Active Volume,” *Nano Lett.*, vol. 18, no. 2, pp. 1075–1081, 2018.
[18] E. Li, B. A. Nia, B. Zhou, and A. X. Wang, “Transparent conductive oxide-gated silicon microring with extreme resonance wavelength tunability,” *Photonics Res.*, vol. 7, no. 4, p. 473, 2019.
[19] C. Argyropoulos, P. Y. Chen, G. D’Aguanno, N. Engheta, and A. Alù, “Boosting optical nonlinearities in ε-near-zero plasmonic channels,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 85, no. 4, pp. 1–5, 2012.
[20] S. Campione, I. Brener, and F. Marquier, “Theory of epsilon-near-zero modes in ultrathin films,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 91, no. 12, pp. 1–5, 2015.
[21] A. P. Vasudev, J.-H. Kang, J. Park, X. Liu, and M. L. Brongersma, “Electro-optical modulation of a silicon waveguide with an ‘epsilon-near-zero’ material,” *Opt. Express*, vol. 21, no. 22, p. 26387, 2013.
[22] H. W. Lee *et al.*, “Nanoscale conducting oxide PlasMOStor,” *Nano Lett.*, vol. 14, no. 11, pp. 6463–6468, 2014.
[23] Q. Gao *et al.*, “Ultra-compact and broadband electro-absorption modulator using an epsilon-near-zero conductive oxide,” *Photonics Res.*, vol. 6, no. 4, p. 277, 2018.
[24] Z. Lu, W. Zhao, and K. Shi, “Ultracompact electroabsorption modulators based on tunable epsilon-near-zero-slot waveguides,” *IEEE Photonics J.*, vol. 4, no. 3, pp. 735–740, 2012.
[25] M. G. Wood *et al.*, “Gigahertz speed operation of epsilon-near-zero silicon photonic modulators,” *Optica*, vol. 5, no. 3, p. 233, 2018.
[26] Y. Gui *et al.*, “Towards integrated metatronics: a holistic approach on precise optical and electrical properties of Indium Tin Oxide,” *Sci. Rep.*, vol. 9, no. 1, pp. 1–10, 2019.
[27] J. H. Park, C. Buurma, S. Sivananthan, R. Kodama, W. Gao, and T. A. Gessert, “The effect of post-annealing on Indium Tin Oxide thin films by magnetron sputtering method,” *Appl. Surf. Sci.*, vol. 307, pp. 388–392, 2014.
[28] Z. Ma, Z. Li, K. Liu, C. Ye, and V. J. Sorger, “Indium-Tin-Oxide for High-performance Electro-optic Modulation,” *Nanophotonics*, vol. 4, no. 1, pp. 198–213, 2015.
[29] J. C. Ranuárez, M. J. Deen, and C. H. Chen, “A review of gate tunneling current in MOS devices,” *Microelectron. Reliab.*, vol. 46, no. 12, pp. 1939–1956, 2006.
[30] Q. Gao, E. Li, and A. X. Wang, “Comparative analysis of transparent conductive oxide electro-absorption modulators [Invited],” *Opt. Mater. Express*, vol. 8, no. 9, p. 2850, 2018.
[31] G. V. Naik, V. M. Shalaev, and A. Boltasseva, “Alternative plasmonic materials: Beyond gold and silver,” *Adv. Mater.*, vol. 25, no. 24, pp. 3264–3294, 2013.
[32] Q. Gao, E. Li, B. Zhou, and A. X. Wang, “Hybrid silicon-conductive oxide- plasmonic electro-absorption modulator with 2-V swing voltage,” *J. Nanophotonics*, vol. 13, no. 3, p. 036005, 2019.
[33] G. V Naik, J. Kim, and A. Boltasseva, “Oxides and nitrides as alternative plasmonic materials in the optical range,” *Opt. Mater. Express*, vol. 1, no. 6, pp. 1090–1099, 2011.
[34] W. R. Veazey and C. D. Hodgman, *Handbook of chemistry and physics*, vol. 7. Chemical Rubber Publishing Company, 1919.
[35] Q. Gao, S. Liverman, and A. X. Wang, “Design and Characterization of High Efficiency Nanoantenna Couplers with Plasmonic Integrated Circuit,” *J. Light. Technol.*, vol. 35, no. 15, pp. 3182–3188, 2017.
[36] X. Xu, J. Covey, D. Kwong, R. T. Chen, H. Subbaraman, and A. Hosseini, “Complementary metal-oxide-semiconductor compatible high efficiency subwavelength grating couplers for silicon integrated photonics,” *Appl. Phys. Lett.*, vol. 101, no. 3, 2012.
[37] S. Campione *et al.*, “Submicrometer Epsilon-Near-Zero Electroabsorption Modulators Enabled by High-Mobility Cadmium Oxide,” *IEEE Photonics J.*, vol. 9, no. 4, 2017.
[38] F. Fuchs and F. Bechstedt, “Indium-oxide polymorphs from first principles: Quasiparticle electronic states,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 77, no. 15, pp. 1–10, 2008.
[39] A. Chaoumead, H. D. Park, B. H. Joo, D. J. Kwak, M. W. Park, and Y. M. Sung, “Structural and electrical properties of titanium-doped indium oxide films deposited by RF sputtering,” *Energy Procedia*, vol. 34, pp. 572–581, 2013.

0733-8724 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: OREGON STATE UNIV. Downloaded on May 03,2020 at 00:41:14 UTC from IEEE Xplore. Restrictions apply.